I. General Information: Instructors and Course  
Sections 201 and 202 Instructor: Prof. Tricia Chigan  
Office Location: BL 401  
Office hours: Monday, Wednesday: 10:00am-11:00am and 1:00pm-2:00pm  
Phone: (978) 934-3364  
E-mail: Tricia_Chigan@uml.edu  
Lecture meeting time & location: Section 201: Monday, Wednesday, Friday 9:00 am-9:50 am in Southwick Hall 407  
Section 202: Monday, Wednesday, Friday 11:00 am-11:50 am in Southwick Hall 407

Section 203 & 204 Instructor: Prof. Jianxin Tang  
Office Location: BL 311  
Office hours: Monday, Wednesday: 1:00pm-2:00pm and 3:00pm-4:00pm  
Phone: (978) 934-5463  
E-mail: Jianxin_Tang@uml.edu  
Lecture meeting time & location: Section 203: Monday, Wednesday, Friday 12:00pm-12:50pm in Kitson 305  
Section 204: Monday, Wednesday, Friday 2:00pm-2:50pm in Kitson 305

Pre-requisites: (1) MATH 1320 Calculus II with a grade of C or better.  
OR (2) COMP 1020 Computing II.

Students for whom the course is intended:  
This is a required course for all Electrical & Computer Engineering, Computer Science, and  
Mechanical Engineering (Robotics option) majors. Students in the Electrical Engineering and  
Computer Engineering graduate programs can also take this course to make up deficiency.

Course web-page: http://faculty.uml.edu/Tricia_Chigan/Courses/16_265/LogicDesign.html

II. Textbook, Notes, Reference, Software  
   Custom Publishing, 2008 (Electronic version is available online, to be announced in class)  
2. Anh Tran, "Experiments in Logic Design", 2014 (To be handed out in week 4)  

III. Course Structure and Goals  
Structure: There are three 50-minute lectures each week. There is also a laboratory component of five  
analysis/designs with software simulation and circuit wiring. Homework exercises will also be assigned  
but not collected/graded.

Goals: This is an introductory course, which covers the basics of digital circuit design in both  
theory and practice. Upon completion of the course, students are expected to be able to:  
1. analyze combinational and sequential circuits,  
2. design/synthesize combinational circuits using SSI and MSI circuits and  
   programmable logic devices,  
3. design/synthesize synchronous sequential circuits,  
4. apply the design techniques of combinational and sequential circuits to the  
   design of more complex circuits using register level logic.

IV. Content Outline  
The contents of the course are partitioned into four parts: fundamentals, combinational logic, sequential  
logic, and register level logic. How they are related to each other and the topics in each part are  
outlined in the chart on p.3. It also shows where the experiments are incorporated into the course.
V. Course Objectives
A. Fundamentals
1. Convert numbers between two systems.
2. Convert numbers to computer codes or vice versa.
3. Generate parity check bits for error detection.
4. Find the 2's complement of signed numbers.
5. Subtract two signed numbers using 2's complement arithmetic.
6. Prove the validity of Boolean equations.
7. Convert and simplify Boolean expressions to SOP and POS by algebraic methods.
8. Minimize the number of literals of a Boolean function.
9. Find the complement and dual of Boolean expressions.
10. Expansion of Boolean functions into sub-functions.
11. Construction of Boolean functions from sub-functions.
12. Represent Boolean functions by binary trees.

B. Combinational Logic
1. Convert Boolean functions to minterm, maxterm, standard SOP & POS forms.
2. Apply active-high and active-low signal levels to circuit inputs and outputs.
3. Apply DeMorgan’s theorem to circuit diagrams without using Boolean algebra.
4. Construct the Karnaugh map for a Boolean function.
5. Use Karnaugh maps to find the simplest SOP & POS for a Boolean function.
6. Recognize the exclusive-OR patterns on a K-map.
7. Partition Karnaugh maps into sub-function maps.
8. Express word problems by truth tables and Boolean functions.
9. Implement a Boolean function as various 2-level circuits.
11. Design combinational circuits using NAND, NOR, AND, OR, XOR.
12. State the functions of decoders, encoders, multiplexers, and demultiplexers.
13. Construct large-size decoders from smaller size decoders.
15. Construct large-size decoders from smaller size decoders.
17. Describe the structures and characteristics of ROM, PLA, & PAL.
18. Implement Boolean functions using programmable logic devices.

C. Sequential Logic
1. Derive the characteristics of SR latches and flip-flops.
2. Derive the characteristic tables, characteristic equations, and state diagrams of various types of flip-flops.
3. State the operations of master-slave flip-flops and edge-triggered flip-flops.
4. Describe the operations of shift registers and counters.
5. Design universal shift registers, self-correcting counters, and ring counters.
6. Describe the difference between the Moore model and the Mealy model of synchronous sequential circuits.
7. Draw the timing diagrams for synchronous sequential circuits.
8. Derive the state diagram of a synchronous sequential circuit by following the analysis procedure.
9. Construct the state diagram of a synchronous sequential circuit.
10. Convert state diagrams to transition tables and next state maps.
11. Derive excitations to flip-flops from next state maps.
12. Design synchronous sequential circuits by following the synthesis procedures.

D. Register Level Logic
1. Partition a more complex circuit into a data path and a control circuit.
2. Describe the operations carried out by a data path.
3. Describe the operations of an algorithmic state machine (ASM) chart.
4. Convert state diagrams to ASM charts.
5. Design using one flip-flop per state.
6. Design state generators.
7. Design the control circuit.
8. Determine the functions performed by an arithmetic processor.
VI. Laboratory Structure:
There are five experiments in this course. Circuit(s) designed in each experiment are simulated by using the software package LogicWorks 4 or LogicWorks 5.0. Circuits can be designed at home or in the computer laboratory (Ball 420) where LogicWorks 4 is available. LogicWorks 4 is also available on vlabs.uml.edu. You can log in with your school credentials. A report is required for each experiment. Students are also required to wire a given combinational circuit in the laboratory using SSI circuits.

Policies:
1. All experiments in this course should be done independently. No collaboration or copying is allowed. Punishments for violating this rule are listed below.
   (i) Report: No credit for the experiment.
   (ii) Design: The letter course grade will be reduced by two levels. For example, a grade of “A” will be reduced to “B+”, “C+” will become “C−”.
   (iii) A letter will be sent to the student’s advisor/department chair/program director.
   Punishment also applies to those who are copied. Therefore safeguard your reports and designs. Do not leave them in public domain.
2. Both the LogicWorks design .cct file and the hard copy of the lab report are due before 2:00 p.m. of the due date. There is a grace period of 48 hours. If the end of the grace period is not on a school day, the grace period is extended to 2:00 p.m. of the next school day. No report will be accepted after the grace period. Exceptions may be granted only by the course instructor under unusual circumstances beyond the control of the student.
3. Circuits that are not designed according to requirements will not be accepted.
4. Additional report and design requirements are described in the laboratory notes.

VII. Calendar and Lecture Topics
The course calendar and lecture topics are given on page 5. Note that (a) lecture topics do not necessarily follow the order of the course contents outlined in Section IV, (b) the coverage of each topic may need more or less time than what is allocated. Thus it is the responsibility of students to attend classes and find out the exact coverage of the course materials in each class.

When class is cancelled or school is closed due to adverse weather or any other reasons, the make-up schedules for examinations will be announced separately. In such cases, the due day for experiments will be extended to the next school day. The wiring of circuits will be re-scheduled. You may call 978-934-2121 for a recorded announcement of class cancellation.

VIII. Course Grade
The distribution of grades is given below. The grade policies for laboratory are described separately in Section VI.

<table>
<thead>
<tr>
<th>Laboratory</th>
<th>Circuit wiring</th>
<th>2%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Experiments 1 &amp; 5</td>
<td>10%</td>
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<tr>
<td>Experiments 2, 3, &amp; 4</td>
<td>18%</td>
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<tr>
<td>Examinations 1</td>
<td>20%</td>
<td></td>
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<tr>
<td>Examinations 2</td>
<td>20%</td>
<td></td>
</tr>
<tr>
<td>Final Exam</td>
<td>25%</td>
<td></td>
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<tr>
<td>Class attendance</td>
<td>5%</td>
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</table>

Attendance is mandatory. The calculation of the grade for attendance is based on the following formula.

Overall grade for attendance

\[
= \frac{\text{Total number of classes student attended}}{(0.80*\text{total number of classes attendance taken})}
\]

“Attending a class” is defined as “presence for a full lecture of 50 minutes”. An index of 0.8 is factored in the formula. A student may miss 20% of the classes due to conditions beyond his/her control such as sickness, etc., but still get full credits for attendance. The maximum overall grade is 100 points. A minimum standard of 60% in the combined experiment and examination grades is used as a measure for the passing of the course. Assignments of course (letter) grades other than "F" depend on class distributions, which usually start with a minimum of 90% for "A".

A course grade of F will be assigned for cheating in exams. A letter will be sent to the student’s advisor/department chair/program director.
### Calendar and Lecture Topics

<table>
<thead>
<tr>
<th>Week</th>
<th>Dates</th>
<th>Lecture Topics (Chapter)</th>
<th>Laboratory/Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>09/05 (W)</td>
<td>Introduction to digital systems. (1)</td>
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<tr>
<td></td>
<td>09/07 (F)</td>
<td>Number systems. (2)</td>
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<tr>
<td>2</td>
<td>09/10 (M)</td>
<td>Number systems and codes. (2)</td>
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<td></td>
<td>09/12 (W)</td>
<td>Boolean algebra. (3)</td>
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<td></td>
<td>09/14 (F)</td>
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<tr>
<td>3</td>
<td>09/17 (M)</td>
<td>Boolean algebra (3)</td>
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<tr>
<td></td>
<td>09/19 (W)</td>
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<td></td>
<td>09/21 (F)</td>
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<td>4</td>
<td>09/24 (M)</td>
<td>Boolean functions and digital circuits (4)</td>
<td>Experiments handouts distributed</td>
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<tr>
<td></td>
<td>09/26 (W)</td>
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<td></td>
<td>09/28 (F)</td>
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<td>5</td>
<td>10/01 (M)</td>
<td>Boolean functions and digital circuits (4)</td>
<td>10/08 Columbus Day</td>
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<td></td>
<td>10/03 (W)</td>
<td>Examination 1 (Friday 10/05, 6:30 pm – 8:00 pm)</td>
<td>Experiment 1 due Wednesday, 10/10</td>
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<td></td>
<td>10/05 (F)</td>
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<tr>
<td>6</td>
<td>10/10 (W)</td>
<td>Karnaugh maps (5)</td>
<td>10/08 Columbus Day</td>
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<td>10/11 (Th)</td>
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<td>Experiment 2 due Wednesday, 10/24</td>
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<td></td>
<td>10/12 (F)</td>
<td></td>
<td>Circuit wiring</td>
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<tr>
<td>7</td>
<td>10/15 (M)</td>
<td>Synthesis of combinational circuits (6)</td>
<td>Experiment 3 due Wednesday, 11/07</td>
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<td></td>
<td>10/17 (W)</td>
<td>Decoders and encoders (7)</td>
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<td></td>
<td>10/19 (F)</td>
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<tr>
<td>8</td>
<td>10/22 (M)</td>
<td>Multiplexers and de-multiplexers (7)</td>
<td>Experiment 2 due Wednesday, 10/24</td>
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<td></td>
<td>10/24 (W)</td>
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<td>10/26 (F)</td>
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<td>9</td>
<td>10/29 (M)</td>
<td>Latches and flip-flops (9)</td>
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<td></td>
<td>10/31 (W)</td>
<td>Shift registers &amp; counters (10)</td>
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<td>11/02 (F)</td>
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<td>10</td>
<td>11/05 (M)</td>
<td>Analysis and synthesis of sequential circuits (10)</td>
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<td>11/07 (W)</td>
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<td></td>
<td>11/09 (F)</td>
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<td></td>
<td>11/16 (F)</td>
<td>Examination 2 (Friday 11/16, 6:30 – 8:00 pm)</td>
<td>11/14- Last day to withdraw with “W”</td>
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<tr>
<td>12</td>
<td>11/19 (M)</td>
<td>Control circuit and data path (11)</td>
<td>11/21-23: Thanksgiving Recess</td>
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<tr>
<td>13</td>
<td>11/26 (M)</td>
<td>Control circuit and data path (11)</td>
<td>Experiment 4 due Monday, 11/26</td>
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<td></td>
<td>11/28 (W)</td>
<td>Design of an arithmetic processor (11)</td>
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<td></td>
<td>11/30 (F)</td>
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<tr>
<td>14</td>
<td>12/03 (M)</td>
<td>Design of an arithmetic processor (11)</td>
<td>Experiment 5 due Friday, 12/07</td>
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<tr>
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<td>12/05 (W)</td>
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<td>12/07 (F)</td>
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<tr>
<td>15</td>
<td>12/10 (M)</td>
<td>Design with ROM, PLA, &amp; PAL (8)</td>
<td>Review</td>
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<td></td>
<td>12/12 (W)</td>
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<tr>
<td>16</td>
<td>Final</td>
<td>Date, time, and room to be announced</td>
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<td></td>
<td>Examination</td>
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</tbody>
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