Introduction to Phase Locked Loop (PLL)

DIGITAVID, Inc.
Ahmed Abu-Hajar, Ph.D.
abuhajar@digitavid.net
Presentation Outline

- What is Phase Locked Loop (PLL)
- Basic PLL System
- Problem of Lock Acquisition
- Phase/Frequency Detector (PFD)
- Charge Pump PLL
- Application of PLL
What is Phase Locked Loop (PLL)

- PLL is an *Electronic Module* (Circuit) that locks the *phase* of the output to the input.
Locked Vs. Unlocked Phase

- Example of locked phase
  \[ V_i(t) \]
  \[ V_o(t) \]

- Example of unlocked phase
  \[ V_o(t) \]
  \[ V_i(t) \]
  \[ \text{Phase Error (\( \Delta \phi \))} \]
Basic PLL System

- PLL is a **feedback** system that **detects** the phase error $\Delta \phi$ and then **adjusts** the phase of the output.

- The Phase Detector (PD), detects $\Delta \phi$ between the output and the input through feedback system.

- Voltage Control Oscillator (VCO) adjusts the phase difference.
Implementation of PD

Phase Detector is an XOR gate

\[ \Delta \phi = \begin{cases} 
1 & V_I \neq V_o \\
0 & V_I = V_o 
\end{cases} \]

\( V_I(t) \)
\( V_o(t) \)

Phase Error \((\Delta \phi)\)
What is VCO?

- VCO is a circuit module that oscillates at a controlled frequency $\omega$.
- The **Oscillating Frequency** is controlled using Voltage $V_{\text{Control}}$.
  - That is why the module is called **Voltage Control Oscillator**

- $V_{\text{control}}$ must be in the **steady state** for the VCO to operate properly

\[ \omega = \omega_0 + K_{\text{VCO}} V_{\text{Control}} \]
Simple PLL

- **Structure**
  - Phase Detector (XOR) that detects the phase error $\Delta \phi$
  - Low Pass Filter (to smooth $\Delta \phi$)
  - Voltage Control Oscillator (VCO)

- **Basic Idea**
  - If $V_i$ and $V_{out}$ are out of phase (unlocked), then the PD module detects the error and the LPF smoothes the error signal. The control signal slows down or speeds up the VCO module; hence, the phase is corrected (locked)
Locked Condition

- Locked Condition

\[
\frac{d}{dt}(\varphi_{in} - \varphi_{out}) = 0
\]

- This implies that

\[
\omega_{in} = \omega_{out}
\]
Example: In the **UNLOCKED** State

- $V_i$ and $V_{out}$ has $\Delta \phi$ at the same frequency $\omega_1$
- The phase detector must produce $V_i$
- Hence, VCO is dynamically changing and PD is creating $V_{Control}$ to adjust for the phase difference.
- The PLL is in the **Locked** state
In the UNLOCKED State

- For Simplicity and by using Fourier Series

- Let \( V_I = V_A \cos(\omega_1 t) \quad V_{out} = V_B \cos(\omega_1 t + \phi_o) \)

- Due to \( \Delta \phi \), PD creates \( V_{control} \)
- VCO will change

\[
\omega_{out} = \omega_1 + K_{VCO} V_{control}
\]

- The output voltage becomes

\[
V_{out} = V_B \cos(\omega_1 t + \phi_o - \Delta \phi(t))
\]
Dynamics of Simple PLL

- PLL is a feedback system
  - PD is a gain amplifier
  - LPF be first order filter (as an example)
  - VCO is a unit step module
- The transfer function of the feedback system is given as:

\[
H(s) = \frac{\Phi_{out}(s)}{\Phi_{in}(s)} = \frac{\omega_{out}(s)}{\omega_{in}(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}
\]

\[
H(s) = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + \omega_{LPF}s + K_{PD}K_{VCO}\omega_{LPF}}
\]
Transient Response to PLL

- The unit step response to second order system
  - Overdamped
  - Critically damped
  - Underdamped

- Problems with this PLL
  - Settling time Vs. ripple of Vcontor
  - Stability of the system
  - Lacks performance in ICs

\[
H(s) = \frac{\Phi_{out}}{\Phi_{in}}(s) = \frac{\omega_{out}}{\omega_{in}}(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}
\]

\[
\Phi = \Phi_{in} + \Phi_{out}
\]
Problem of Lock Acquisition

- When PLL is turned on, the output frequency is far from the input frequency
- It is possible that the PLL would never lock
- Modern PLL uses FREQUENCY DEDECTOR (FD) in addition to the PD.

![PLL Diagram]

\[ V_{in} \quad \omega_{in} \]

\[ PD \quad LPF1 \quad + \quad VCO \quad \]

\[ FD \quad LPF2 \quad \]

\[ V_{out} \quad \omega_{out} \]
Phase/Frequency Detector (PFD)

- One Module that detects both frequency and phase differences
- This module senses the transition in A or B

<table>
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<th>Initially</th>
<th>A</th>
<th>B</th>
<th>QA</th>
<th>QB</th>
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<tr>
<td>A leads B</td>
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<td></td>
<td>A</td>
<td>B</td>
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<td>1</td>
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</tbody>
</table>

- If A leads B, $Q_A$ changes its state and $Q_B$ remains unchanged
- If B leads A, $Q_B$ changes its state and $Q_A$ remains unchanged
Hardware Implementation of PFD

- **Uses two Edge Triggering modules using D-FF**
  - If A leads to “1” $Q_A = “1”$
    - When B becomes “1”, $Q_B = “1”$
      - The AND gate RESETs Both to $Qs “0”$
  - If B leads to “1” $Q_B = “1”$
    - When A becomes “1”, $Q_A = “1”$
      - The AND gate RESETs Both to $Qs “0”$
Hardware Implementation of PFD

The $V_{out}$ is the average of $(Q_A - Q_B)$ is used to detect the phase and the frequency difference.
The Basic Block diagram

- Structure
  - PFD
  - LPF
  - Differential Amplifier
  - VCO
  - Negative Feedback
- **Disadvantage:** Sensitive to noise and offset voltages, ripple $V_{\text{control}}$, ..
- Use Charge Pump PLL
Charge Pump PLL

- **Structure**
  - PFD
  - Two switches controlled by QA and QB
  - Capacitor
    \[ I_c = C \frac{dV_c}{dt} \]
    \[ \frac{dV_c}{dt} = \frac{I_c}{C} \]
  - VCO
  - Negative Feedback
  - It charges or discharges the capacitor indefinitely
Charge Pump PLL

- The capacitor is replaced with a LPF (Cp and Rp) to improve the phase margin for stability.
- The transfer function of the system is approximated as follows:

\[
H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_p} (R_p C_p s + 1)}{s^2 + \frac{I_p}{2\pi} K_{VCO} R_p s + \frac{I_p K_{VCO}}{2\pi C_p} K_{VCO}}
\]

- \( R_p \) slows down the system.
Application of PLL

- Frequency Multiplications
  - The feedback loop has frequency division
  - Frequency division is implemented using a counter

Clock Skew Reduction
- Buffers are used to distribute the clock
- Embed the buffer within the loop
Application of PLL

- Clock Skew Reduction
  - Buffers are used to distribute the clock
  - Embed the buffer within the loop

- Jitter Reduction