17.342 Logic Design II and Lab
Lab 2
Spring 2012

Bit-Sequence Detector

Lab Report

See separate report form located on the Class Web Site. This form should be completed during the performance of this lab.

Objectives

1) To learn the design procedures of Moore model and Mealy model synchronous sequential circuits.

Materials

1) Access to one of the following software packages

   a. "LogicWorks 5: Interactive Circuit Design Software", Addison Wesley, 2004

   b. ... OR ... "LogicWorks 4, Addison Wesley, 1999

   c. ...OR ... SimUaid

WARNINGS AND PRECAUTIONS

1) None

Source File Locations

1. None

Background Information

1. None

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Pre-Lab Preparation

1. Read Units 13 and 14 in the course textbook.

2. Download Lab Report Template provided on the Class Web Site

3. Download templates for the schematic diagrams located on the Class Web Site

Problem description

A synchronous sequential circuit known as a bit-sequence detector (or recognizer) is to be designed.

The detector has one input x and one output Z.

When a specific 5-bit sequence $a_0\, a_1\, a_2\, a_3\, a_4$ inputted to the circuit in five consecutive clock cycles is detected, Z becomes 1. Otherwise Z remains 0. The output returns to 0 when the circuit starts to detect the next sequence.

Overlapping of sequences is not allowed.

An active-high RESET input is used to initialize the circuit.

State minimization is required. State assignment is arbitrary.

Bit-sequence … $a_0\, a_1\, a_2\, a_3\, a_4$ = 0 0 0 1 0

IC Requirements

The maximum number of ICs that can be used in each of your designs is six besides those already in the template for the schematic diagram. ICs should be selected from the following list. There is no limit on the number of ICs that can be used for each type …

IC type 7400 (quadruple 2-input NAND gates)
IC type 7402 (quadruple 2-input NOR gates)
IC type 7410 (triple 3-input NAND gates)
IC type 7420 (dual 4-input NAND gates)
IC type 7486 (quadruple 2-input XOR gates)

Procedure

Design 1. MOORE MACHINE

a. Design a synchronous sequential circuit using JK flip-flops as identified in the problem description.

The circuit will be designed as a Moore Machine.

A LogicWorks template, Schematic 1, is available as a starting point for your design and is available for download on the Class Web Site. The template is also shown in Figure 1.

b. Simulate your design using one of the software packages identified in the materials portion of this lab.

c. Record your work in your Lab Report (template provided on the Class Web Site).

Design 2. MEALY MACHINE

a. Design a synchronous sequential circuit using T flip-flops as identified in the problem description. A T flip-flop can be constructed from a JK flip-flop by connecting J and K together to produce the T excitation. Use 7476 for JK flip-flops.

The circuit will be designed as a Mealy Machine.

A LogicWorks template, Schematic 2, is available as a starting point for your design and is available for download on the Class Web Site. The template is also shown in Figure 2.

b. Simulate your design using one of the software packages identified in the materials portion of this lab.

c. Record your work in your Lab Report (template provided on the Class Web Site).

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SUMMARY:

You have designed two synchronous sequential circuits … one as a Moore Machine, the other as a Mealy Machine. In addition, you simulated both designs to prove that it functioned as required.

Lab Notebook Requirements:

Not required.

Lab Report:

1. Use template provided on the Class Web Site.

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Figure 1
Schematic 1
Bit-Sequence Detector (Moore Machine)

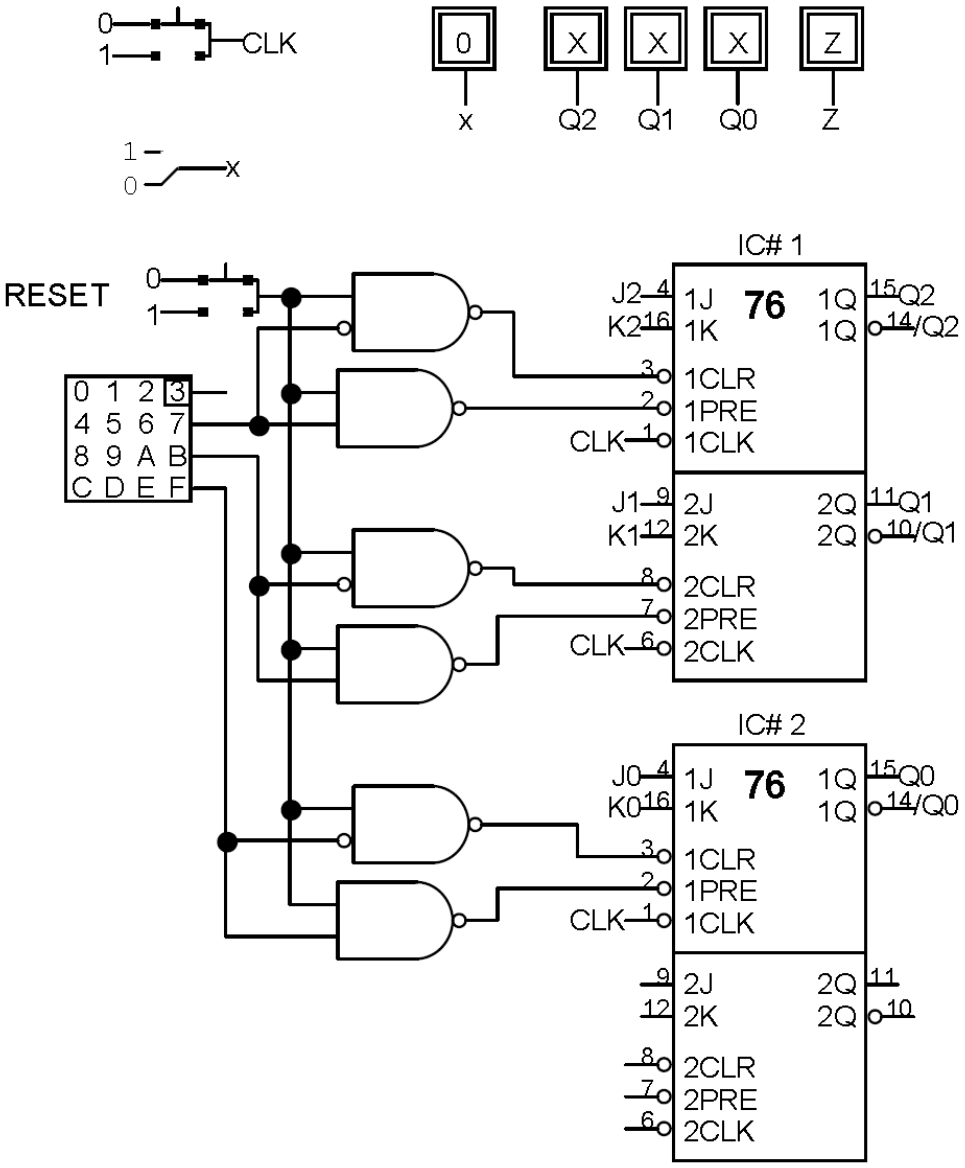

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Figure 2
Schematic 2
Bit-Sequence Detector (Mealy Machine)

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Experiment 2: Bit-sequence detector (Mealy)
Name:
Bit sequence: