Network Processor and Its Applications

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Network Processor Architecture and Applications

- ## Introduction to networking

- ## Network applications
  - IPv4 routing, classification etc. (Traditional)
  - URL-based switching,transcoding, etc. (New)

- ## Network Processor Architectures
  - Cisco Toaster
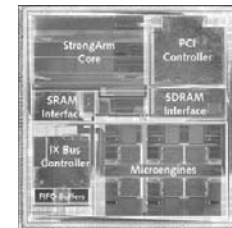 - IBM(Hifn) PowerNP
  - Intel IXP

What the Internet Needs?

Increasing Huge Amount of Packets & Routing, Packet Classification, Encryption, QoS, New Applications and Protocols, etc.....

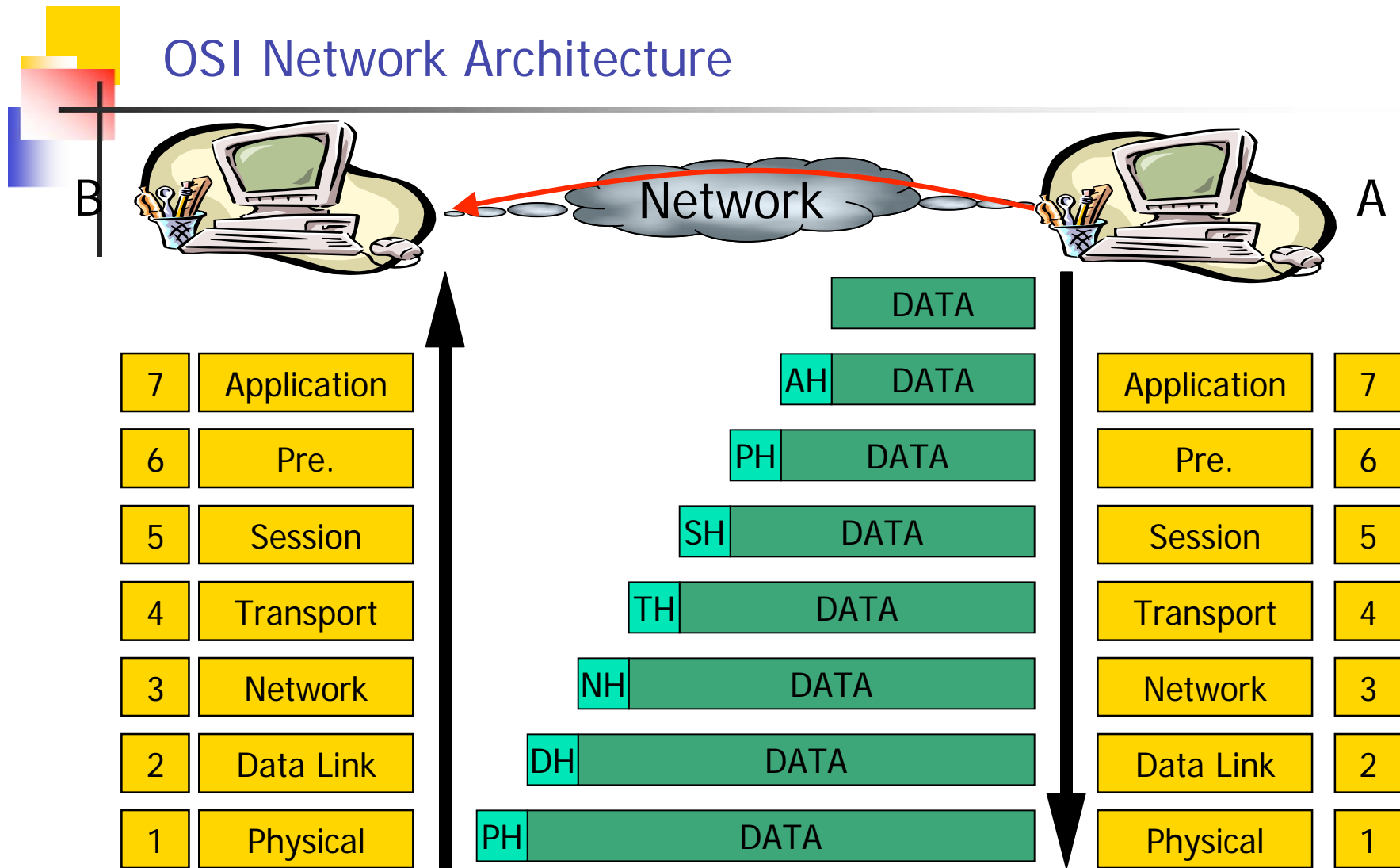**ASIC (large, expensive to develop, not flexible)**

+

General Purpose RISC (not capable enough)

- High processing power
- Support wire speed
- Programmable
- Scalable
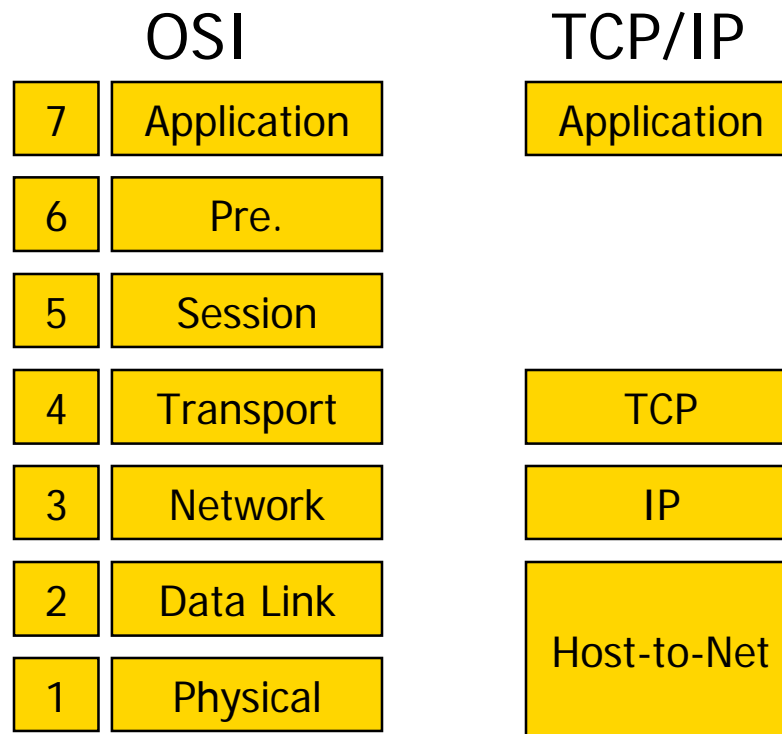- Specially for network applications
- ...

OSI Network Architecture

B   Network   A

				DATA		
7	Application		AH	DATA	Application	7
6	Pre.		PH	DATA	Pre.	6
5	Session		SH	DATA	Session	5
4	Transport		TH	DATA	Transport	4
3	Network		NH	DATA	Network	3
2	Data Link		DH	DATA	Data Link	2
1	Physical		PH	DATA	Physical	1

Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

TCP/IP Model

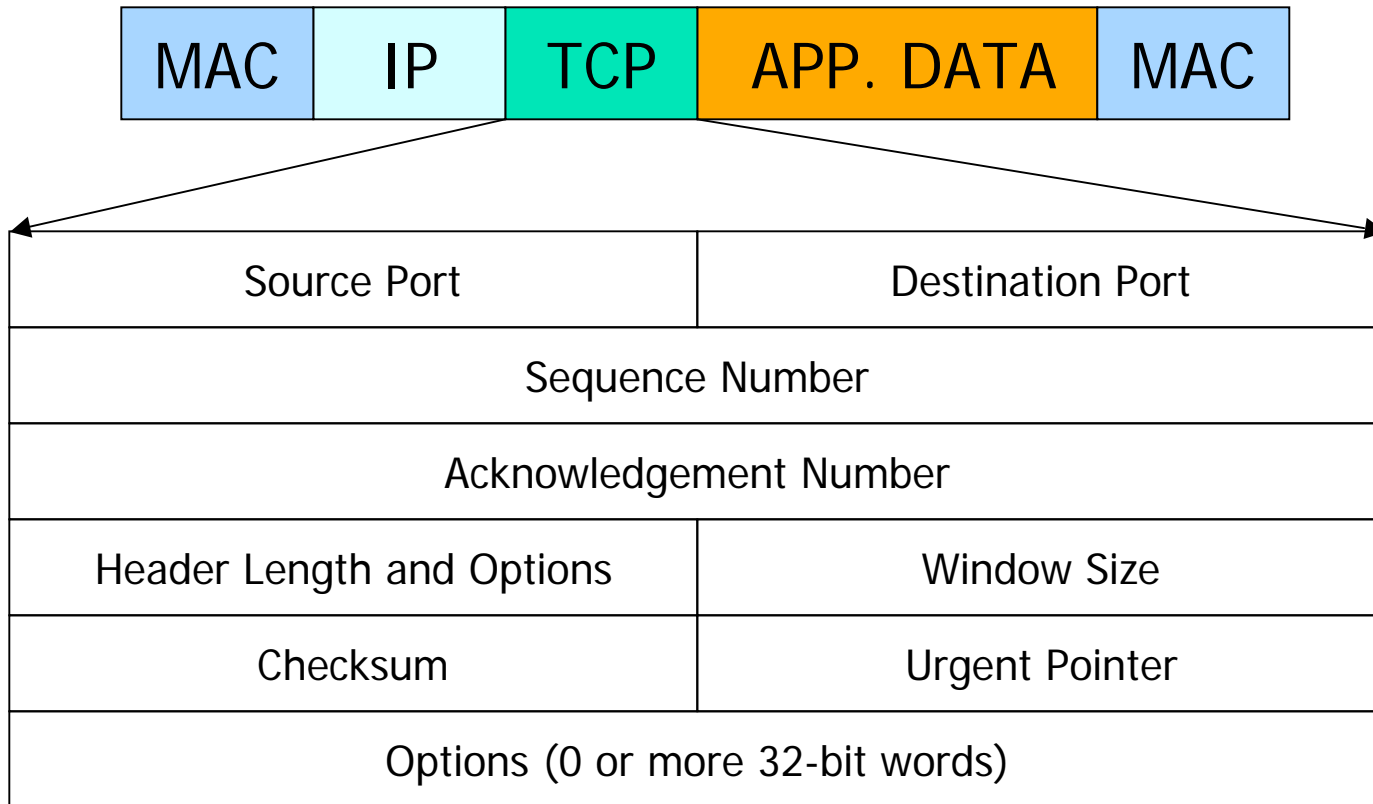|	OSI		TCP/IP
7	Application		Application
6	Pre.		
5	Session		
4	Transport		TCP
3	Network		IP
2	Data Link		Host-to-Net
1	Physical		

Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

- ISO OSI (Open Systems Interconnection) not fully implemented
- Presentation and Session layers not present in TCP/IP

TCP/IP packet

| MAC | IP | TCP | APP. DATA | MAC |

Source Port	Destination Port
Sequence Number	
Acknowledgement Number	
Header Length and Options	Window Size
Checksum	Urgent Pointer
Options (0 or more 32-bit words)	

Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

TCP/IP packet

MAC	IP	TCP	APP. DATA	MAC

Ver.	IHL	Service Type	Total Length
Identification			Options and Fragment Offset
Time to Live		Protocol	Header Checksum
Source Address			
Destination Address			
Options (0 or more 32-bit words)			

Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

TCP/IP packet

MAC	IP	TCP	APP. DATA	MAC

Preamble	D. Add.	S. Add.	Leng.

CRC
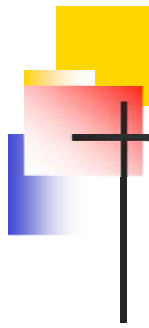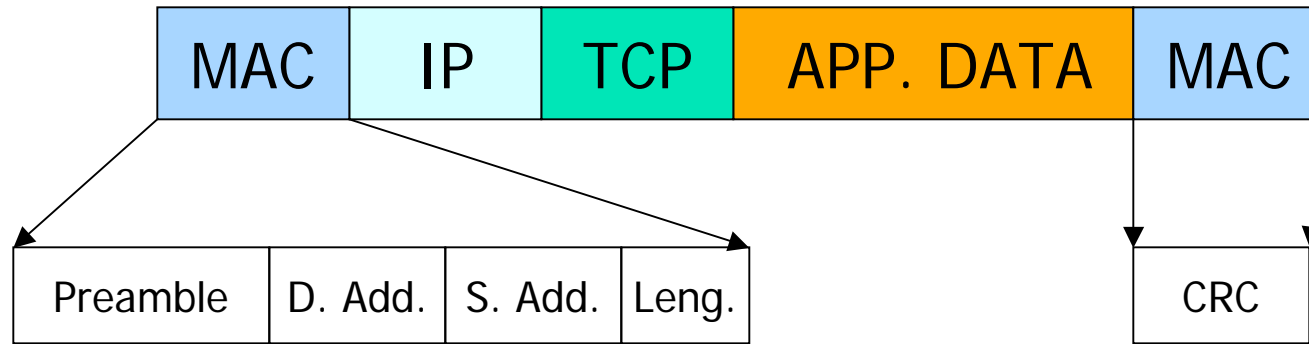
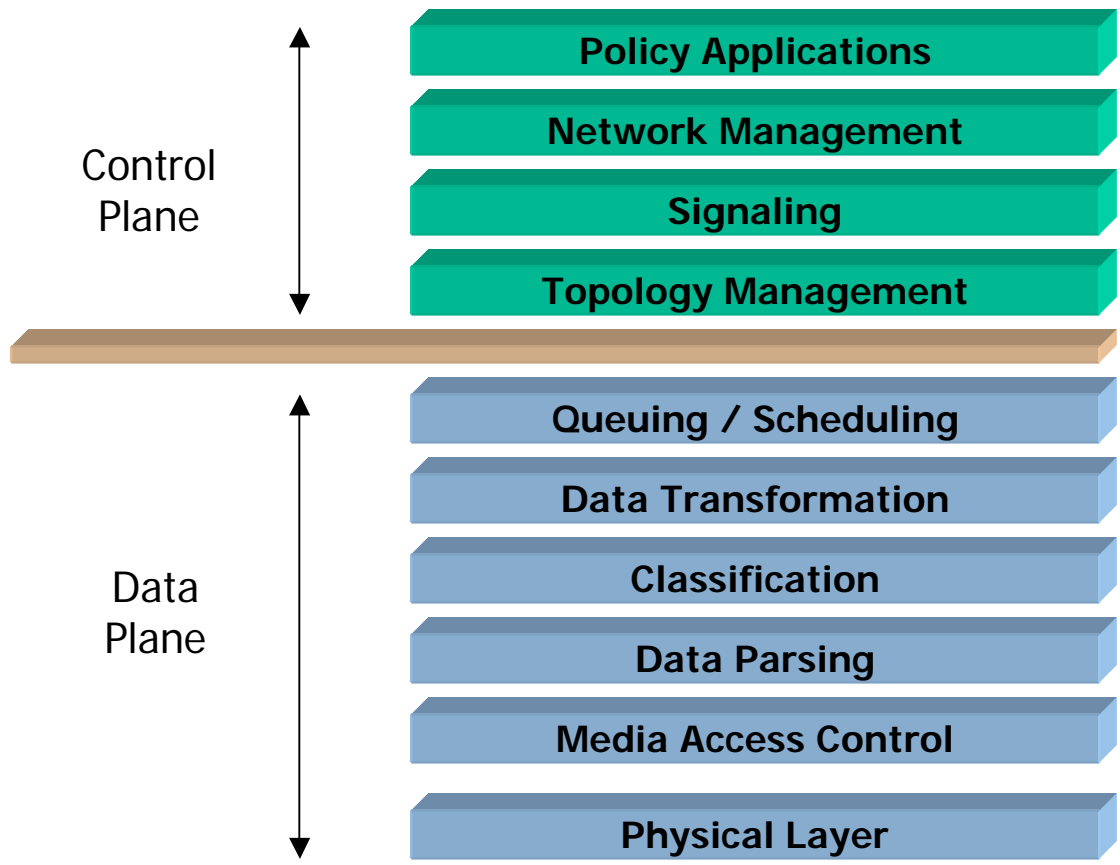Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

Application Categorization

- **Control-Plane tasks**
  - Less time-critical
  - Control and management of device operation
    - Table maintenance, port states, etc.
- **Data-Plane tasks**
  - Operations occurring real-time on "packet path"
  - Core device operations
    - Receive, process and transmit packets
      Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

Processing Tasks

Control Plane

- Policy Applications
- Network Management
- Signaling
- Topology Management

Data Plane

- Queuing / Scheduling
- Data Transformation
- Classification
- Data Parsing
- Media Access Control
- Physical Layer

Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

Data Plane Tasks

- **Media Access Control**
  - Low-level protocol implementation
    - Ethernet, SONET framing, ATM cell processing, etc.

- **Data Parsing**
  - Parsing cell or packet headers for address or protocol information

- **Classification**
  - Identify packet against a criteria (filtering / forwarding decision, QoS, accounting, etc.)

- **Data Transformation**
  - Transformation of packet data between protocols

- **Traffic Management**
 - Queuing, scheduling and policing packet data

Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

Other Network Processor Applications

- ## Routing table lookup
  - Determine the next hop for incoming packets

- ## Packet Classification
  - classify packets using header fields against a set of rules

- ## URL-based Switching
  - Distribute HTTP requests based on URLs.

- ## Transcoding
  - Encryption/Decryption, intrusion detection, firewall, access control checking, denial-of-service
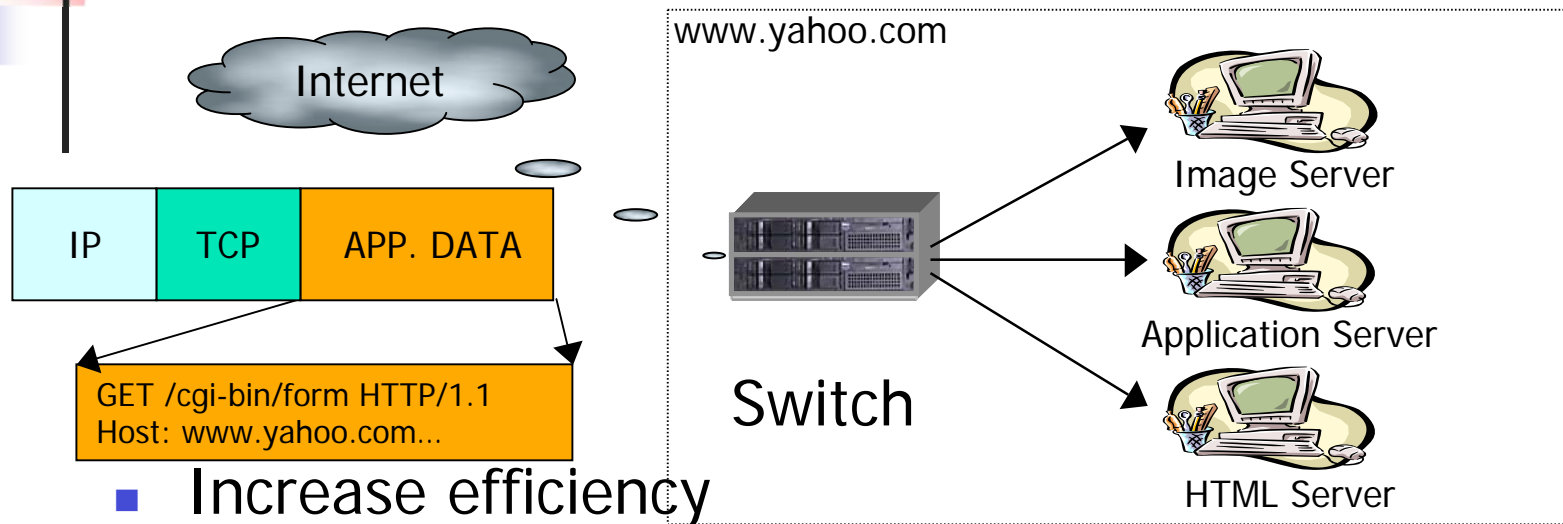
IPv4 Routing
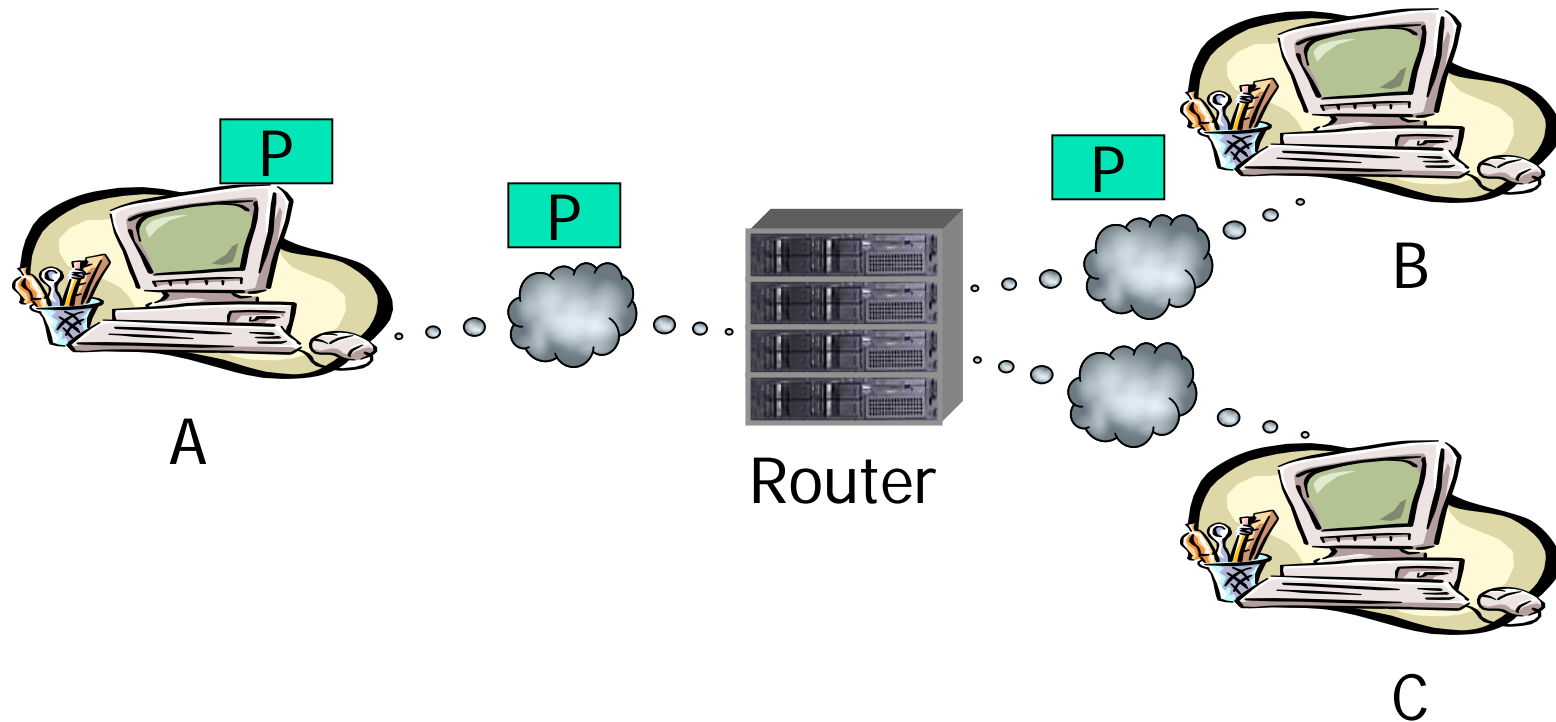
- Routers determine next hop and forward packets

Packet Classification

- Routers are required to distinguish packets for
  - Flow identification
  - Fair sharing of bandwidth
  - QoS
  - Security
  - Accounting, billing
  - etc
- Packets are classified by rules
  - Src IP, Dest IP, src port #, dest port # etc
- Classification Algorithm Metrics
  - Search speed
  - Storage cost
  - Scalability
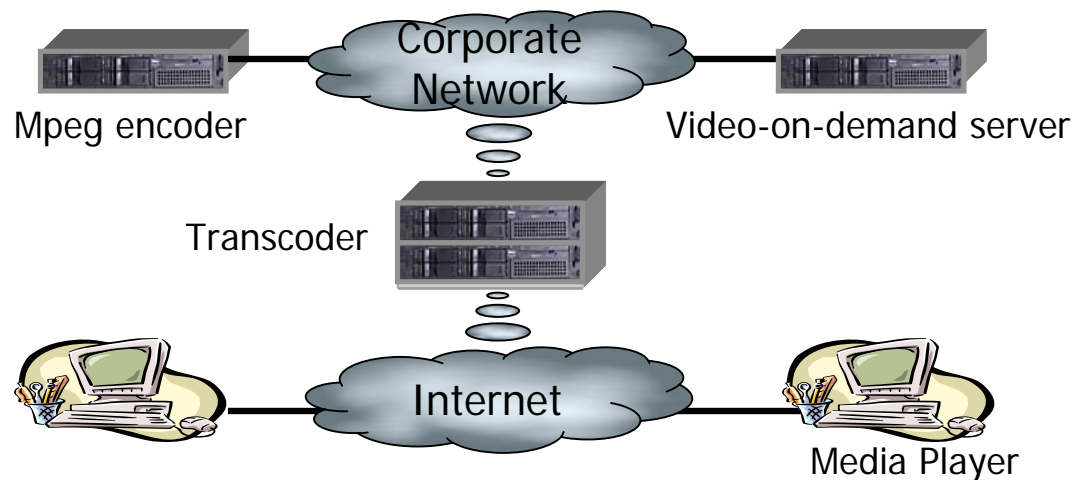 - Updates
  - Etc.

URL-based switching

Internet

www.yahoo.com

IP	TCP	APP. DATA

GET /cgi-bin/form HTTP/1.1
Host: www.yahoo.com...

Switch

Image Server

Application Server

HTML Server

- **Increase efficiency**
- **Tasks**
  - Traverse the packet data (request) for each arriving packet and classify it:
    - Contains '.jpg' -> to image server
    - Contains 'cgi-bin/' -> to application server

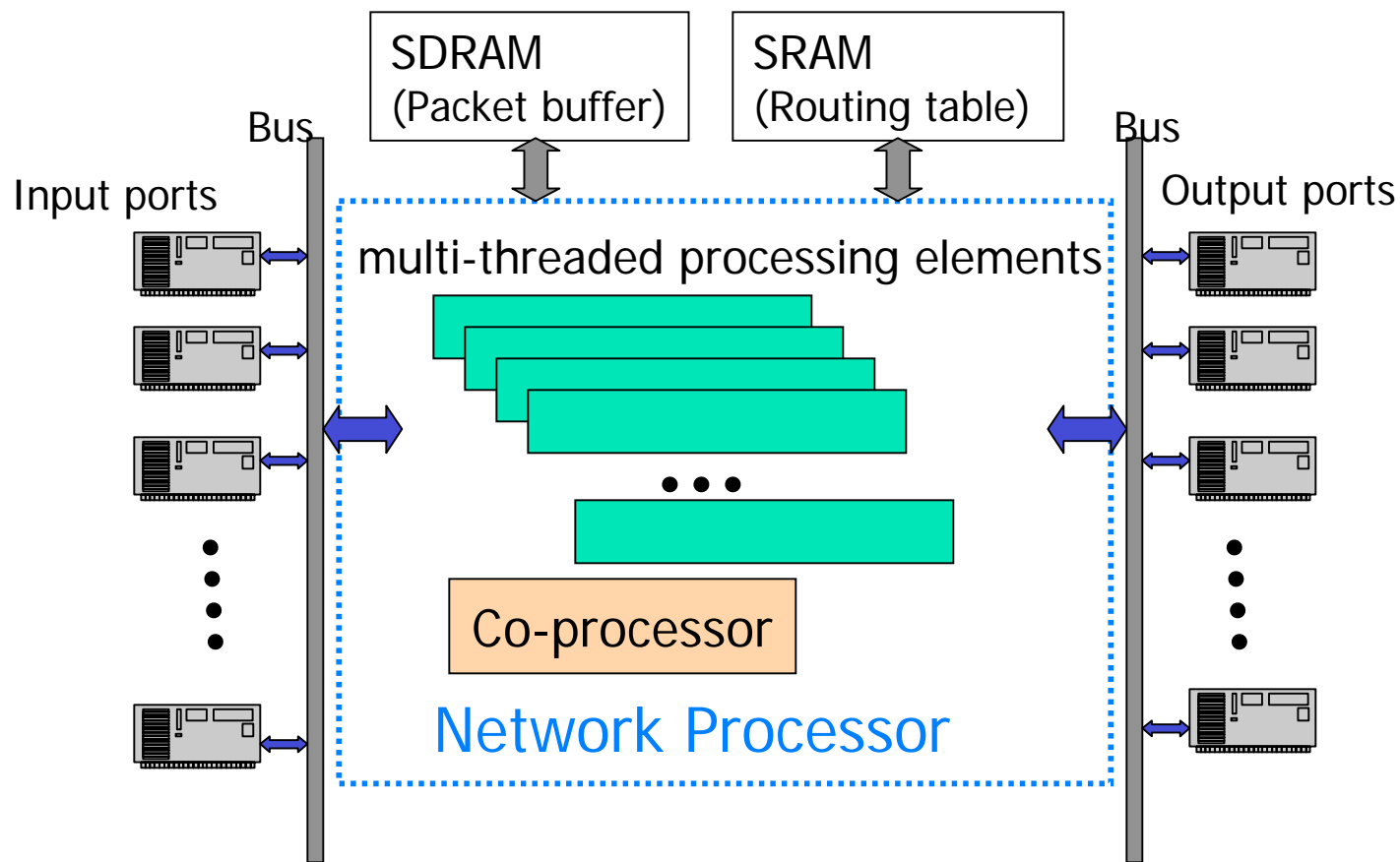Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

Transcoders

- ## Two important requirements
  - ### If the receiver is not capable of interpreting the stored data (multimedia transcoders)
    - wireless receivers, hand-held devices, etc.
  - ### Compression for bandwidth and storage efficiency

Mpeg encoder — Corporate Network — Video-on-demand server

Transcoder

Internet

Media Player

Source: Network Processor Tutorial in Micro 34 - Mangione-Smith & Memik

Typical NP Architecture

SDRAM
(Packet buffer)

SRAM
(Routing table)

Bus

Bus

Input ports

Output ports

multi-threaded processing elements

• • •

Co-processor

Network Processor

Why Network Processors

- **Current Situation**
  - Data rates are increasing
  - Protocols are becoming more dynamic and sophisticated
  - Protocols are being introduced more rapidly
- **Processing Elements**
  - GP(General-purpose Processor)
    - Programmable, Not optimized for networking applications
  - ASIC(Application Specific Integrated Circuit)
    - high processing capacity, long time to develop, Lack the flexibility
  - NP(Network Processor)
    - achieve high processing performance
    - programming flexibility
    - Cheaper than GP

Organizing Processor Resources

- **Design decisions:**
  - High-level organization
  - ISA and micro architecture
  - Memory and I/O integration
- **Today's commercial NPs:**
  - Chip multiprocessors
  - Most are multithreaded
  - Exploit little ILP (Cisco does)
 - No cache
  - Micro-programmed

Example Toaster System: Cisco 10000
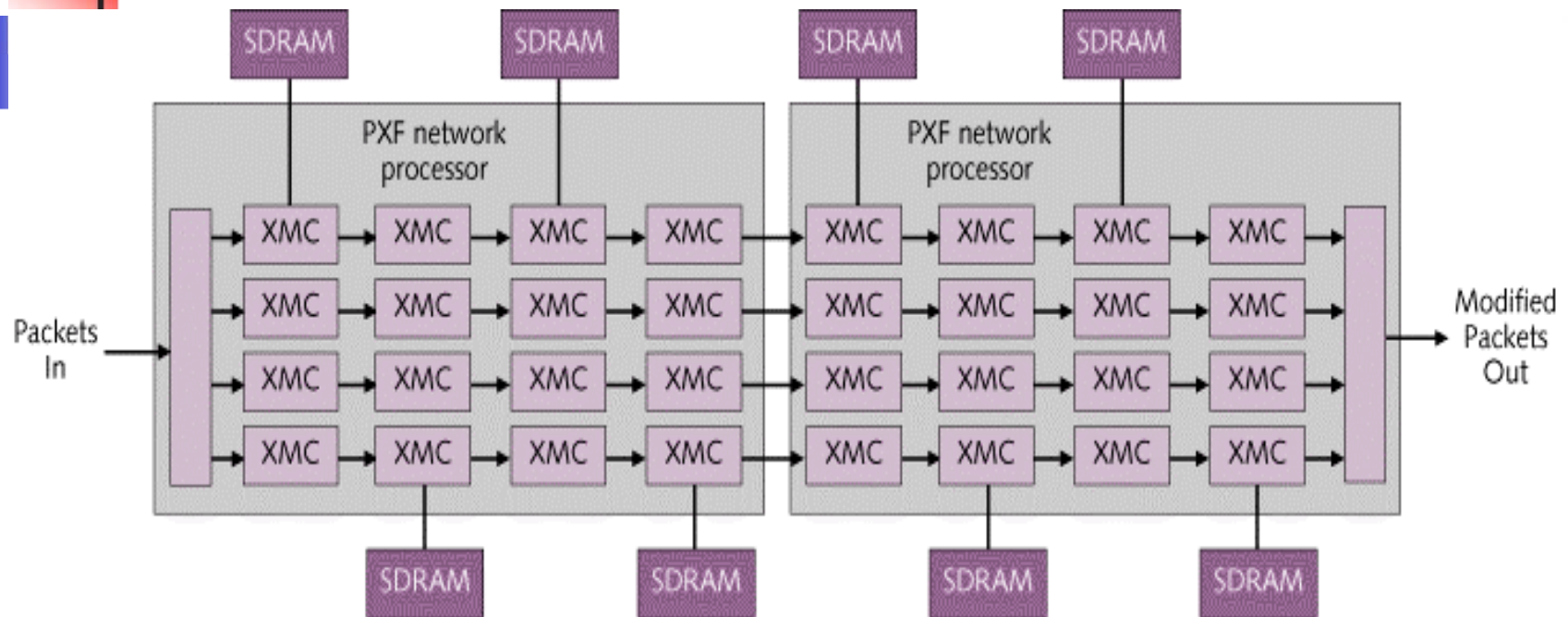
- Almost all data plane operations execute on the programmable XMC
- Pipeline stages are assigned tasks – e.g. classification, routing, firewall, MPLS
  - Classic SW load balancing problem
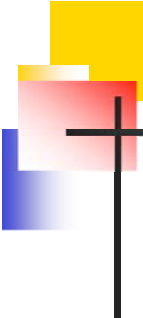- External SDRAM shared by common pipe stages

IBM PowerNP

- 16 pico-procesors and 1 powerPC
- Each pico-processor
  - Support 2 hardware threads
  - 3 stage pipeline : fetch/decode/execute
- Dyadic Processing Unit
  - Two pico-processors
  - 2KB Shared memory
  - Tree search engine
- Focus is layers 2-4
- PowerPC 405 for control plane operations
 - 16K I and D caches
- Target is OC-48
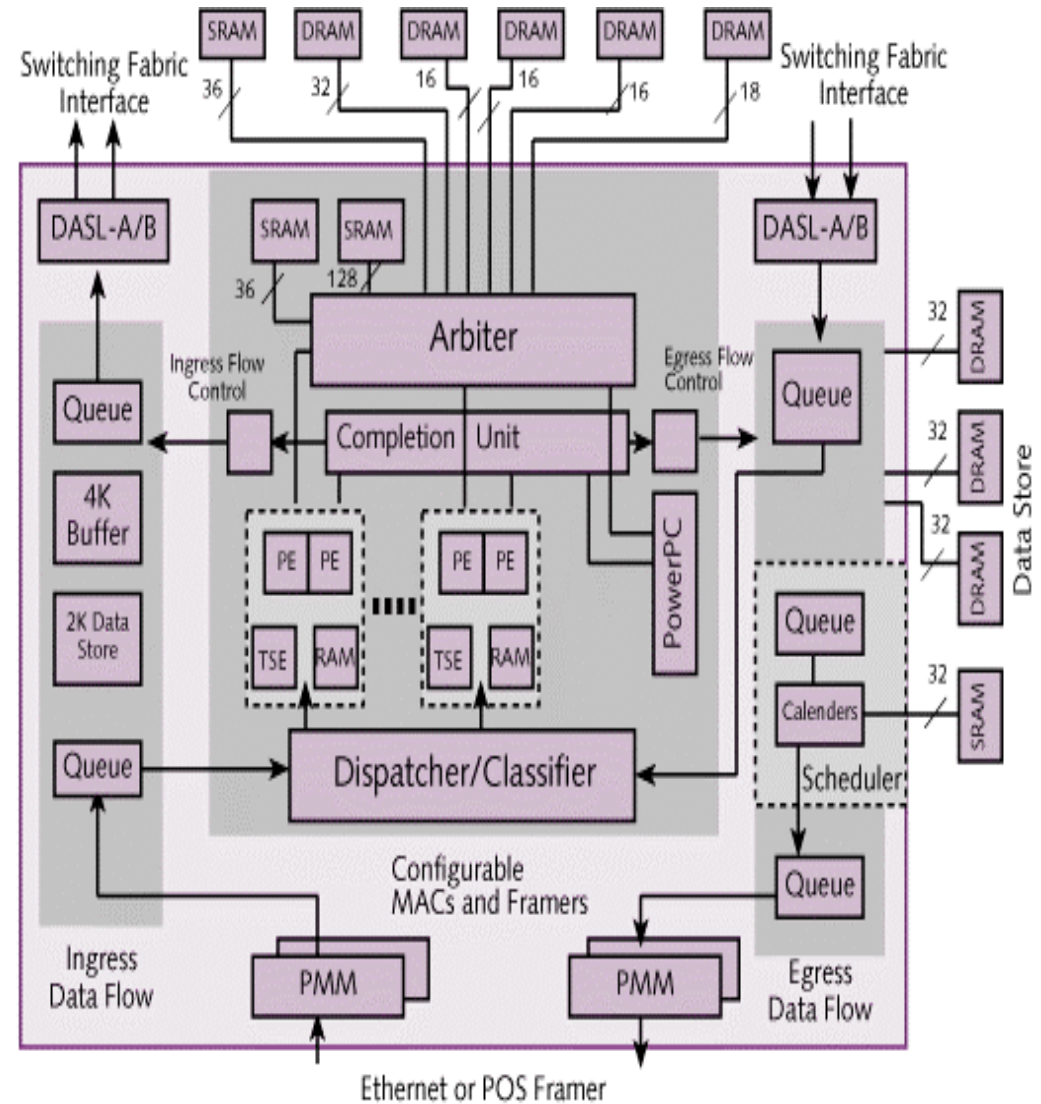
C-Port C-5 Chip Architecture
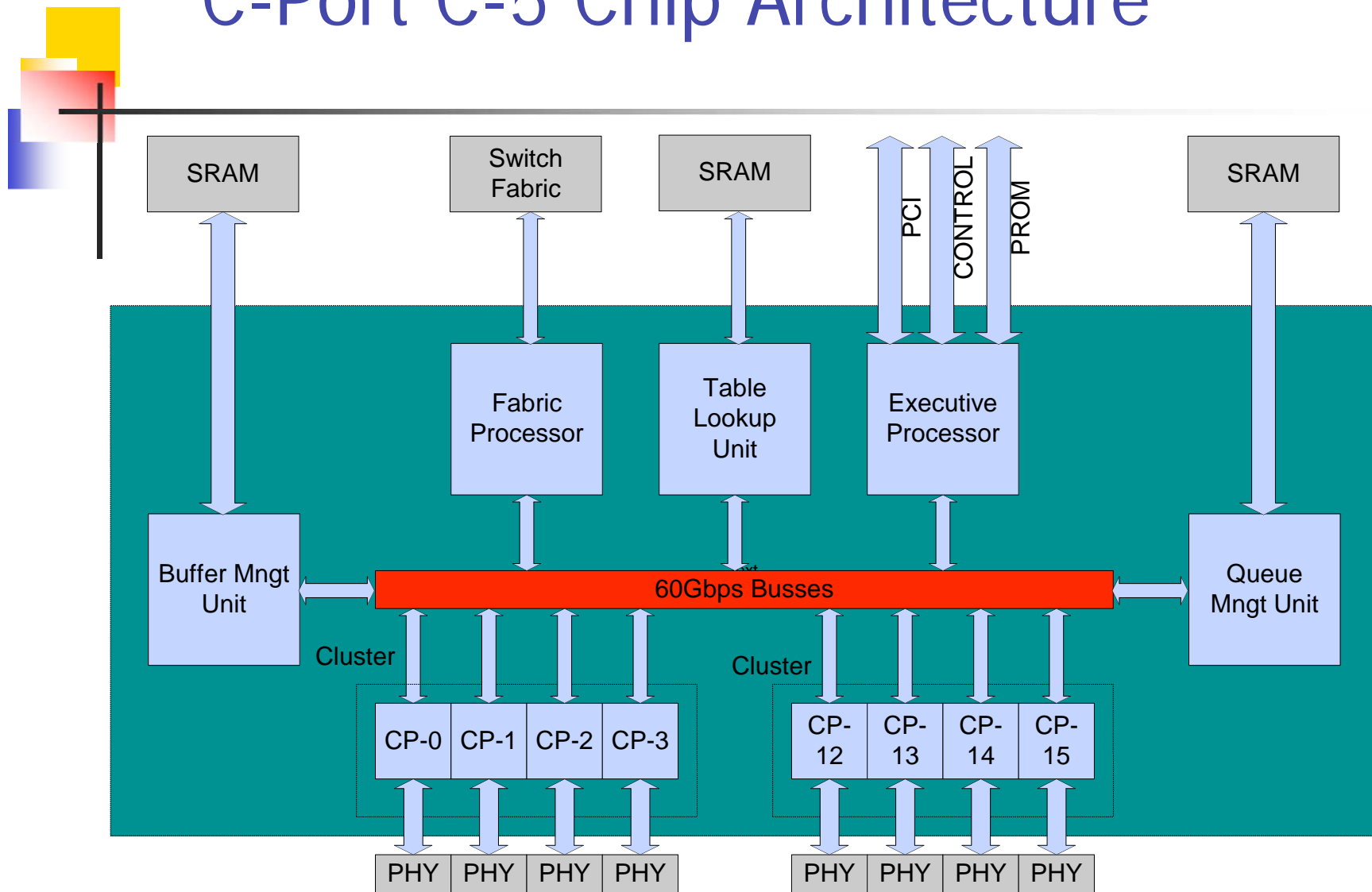
Some Challenges

- **Intelligent Design**
  - Given a selection of programs, a target network link speed, the 'best' design for the processor
    - Least area
    - Least power
    - Most performance
- **Write efficient multithreaded programs**
  - NPs have
    - Heterogeneous computer resources
    - Non-uniform memory
    - Multiple interacting threads of execution
    - Real-time constraints
  - Make use of resources
    - How to use special instructions and hardware assists
      - Compilers
      - Hand-coded
  - Multithreaded programs
    - Manage access to shared state
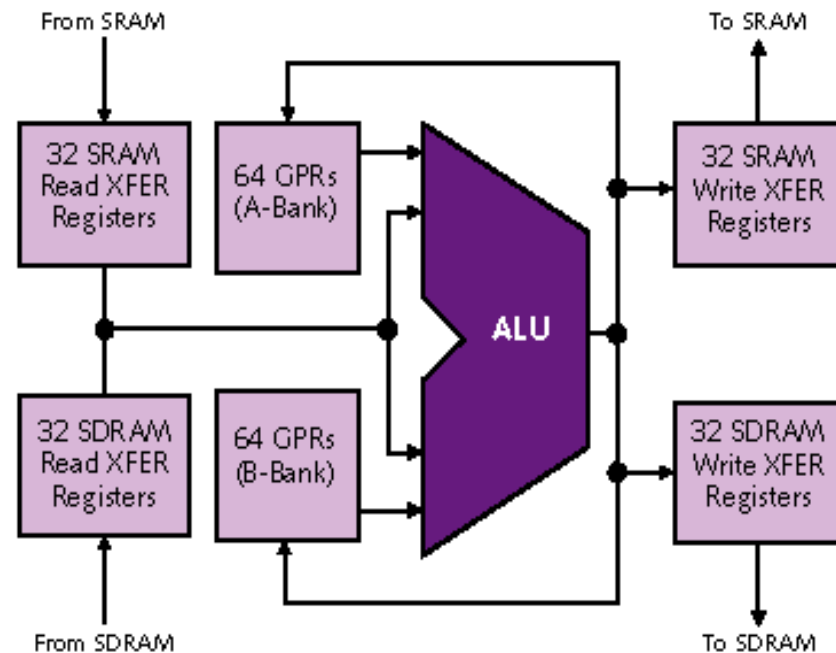   - Synchronization between threads
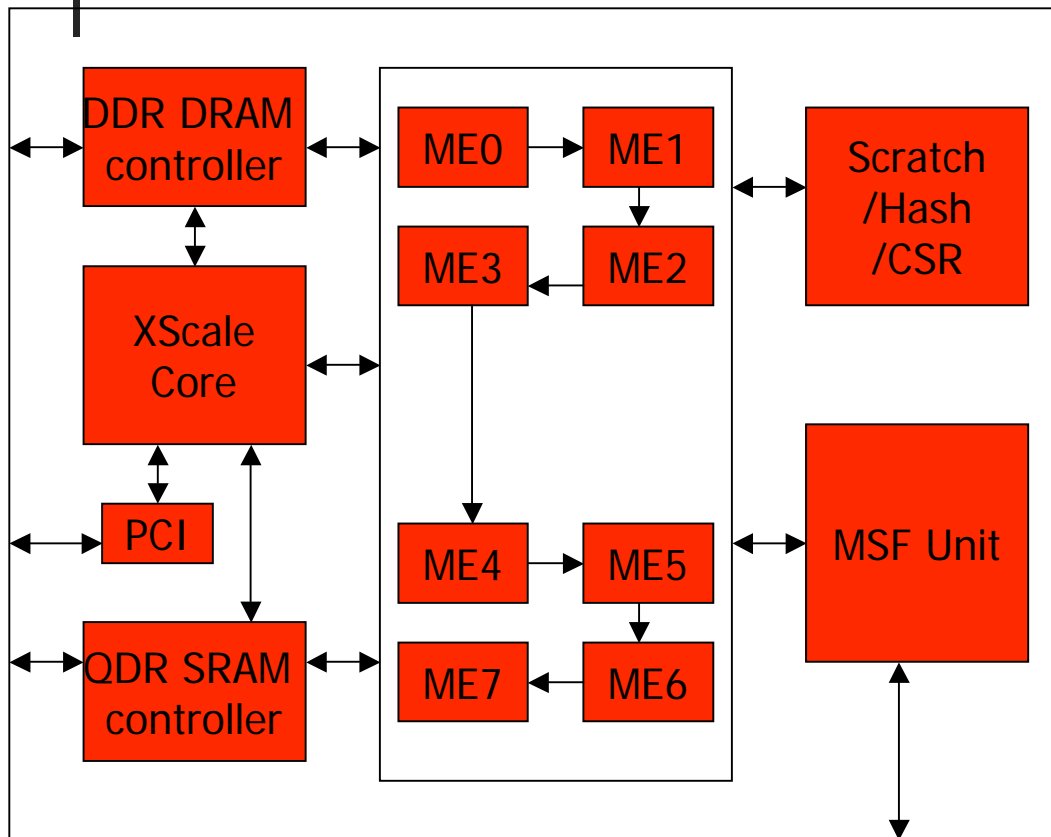
IXP1200 Block Diagram
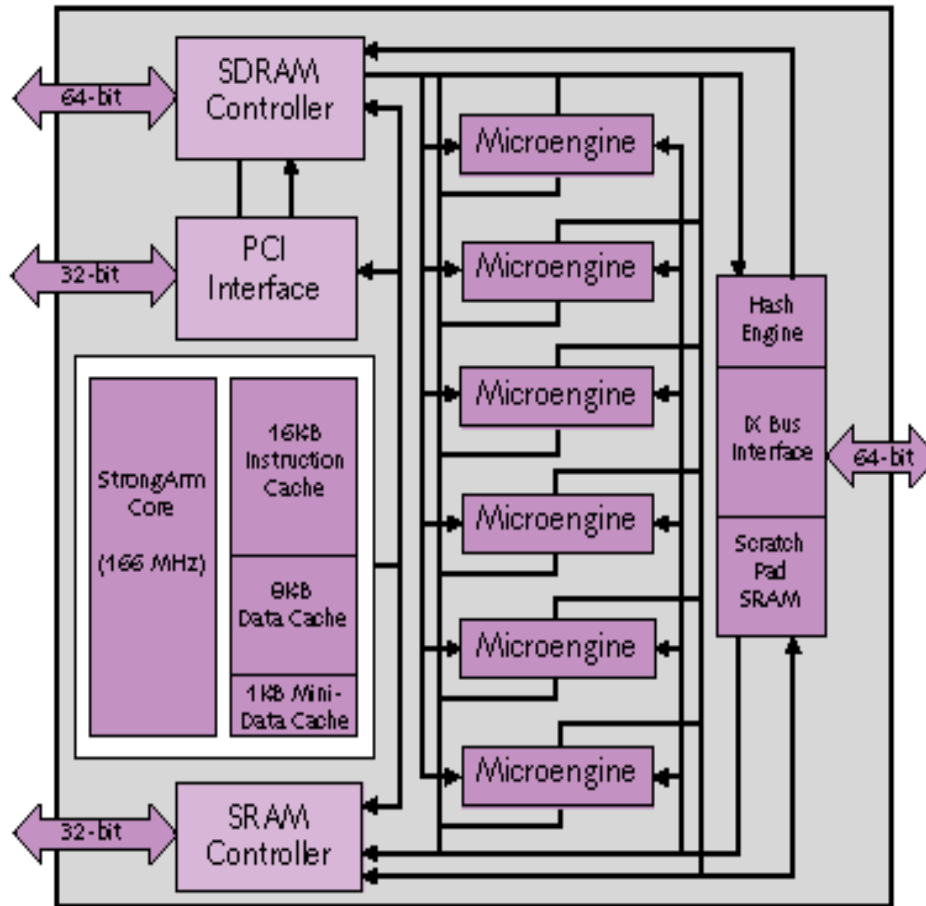
- **StrongARM processing core**
- **Microengines introduce new ISA**
- **I/O**
  - PCI
  - SDRAM
  - SRAM
  - IX : PCI-like packet bus
- **On chip FIFOs**
  - 16 entry 64B each

IXP1200 Microengine

- **4 hardware contexts**
    - Single issue processor
    - Explicit optional context switch on SRAM access
- **Registers**
    - All are single ported
    - Separate GPR
    - 256*6 = 1536 registers total
- **32-bit ALU**
    - Can access GPR or XFER registers
- **Shared hash unit**
    - 1/2/3 values – 48b/64b
    - For IP routing hashing
- **Standard 5 stage pipeline**
- **4KB SRAM instruction store – not a cache!**
- **Barrel shifter**

IXP 2400 Block Diagram

DDR DRAM controller	ME0 → ME1	Scratch /Hash /CSR
	ME3 ← ME2	
XScale Core		
PCI	ME4 → ME5	MSF Unit
QDR SRAM controller	ME7 ← ME6	

- **XScale core replaces StrongARM**
- **Microengines**
  - Faster
  - More: 2 clusters of 4 microengines each
- **Local memory**
- **Next neighbor routes added between microengines**
- **Hardware to accelerate CRC operations and Random number generation**
- **16 entry CAM**

Different Types of Memory

Type	Width (byte)	Size (bytes)	Approx unloaded latency (cycles)	Notes
Local	4	2560	1	Indexed addressing post incr/decr
On-chip Scratch	4	16K	60	Atomic ops
SRAM	4	256M	150	Atomic ops
DRAM	8	2G	300	Direct path to/fro MSF

Ref: [NPRD]

IXA Software Framework

External Processors

Control Plane Protocol Stack

XScale Core

Control Plane PDK

Core Components

Core Component Library

Resource Manager Library

C/C++ Language

Microengine Pipeline

Microblock Library

Micro block → Micro block → Micro block

Protocol Library

Utility Library

Hardware Abstraction Library

Microengine C Language
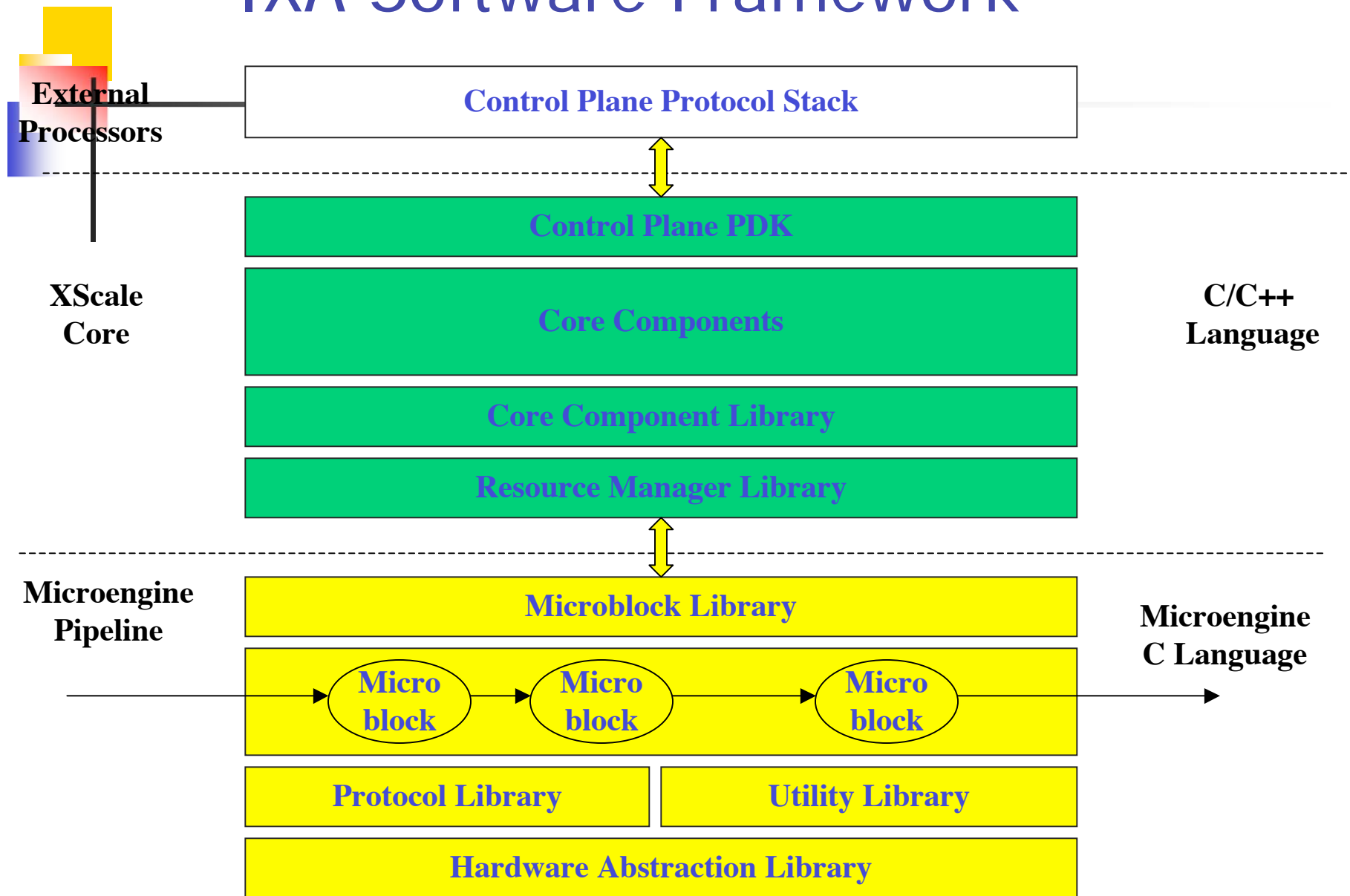
Summary

- ## NP is developing very fast and is a hot research area

- ## Multithreaded NP Architectures provide tremendous packet processing capability

- ## NP can be applied in various network layers and applications

  - Traditional apps – forwarding, classification
  - Advanced apps – transcoding, URL-based switching, security etc.
  - New apps