

Lecture Notes of 16.317

Microprocessor I

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The following lecture notes are available for your convenience. They are NOT complete outlines of lectures. Class attendance is highly recommended.

1. Chapter 1. Introduction to Microprocessor

1. The success of Personal Computers (PCs), open system, 16bit, 32bit
2. I/O, PCI, terminal, file server, LAN, VLSI, MPU
3. General architecture of a microcomputer, primary and secondary storage memory, ROM, RAM.
4. Evolution of Intel processors, performance evaluation, benchmarking, transistor density
5. reprogrammable microprocessor, embedded microprocessor, microcontroller
6. operating systems, memory management, protection, multitasking

2. Chapter 2. Real-mode Software Architecture of 80386DX

1. Describe the internal architecture of 80386DX.
 - execution unit
 - segment unit
 - page unit
 - bus unit
 - prefetch unit
 - decode unit
2. Describe real-mode software architecture: registers, memory space size
3. Describe real-mode memory space and data organization.
 - aligned double-word, unaligned double-word
 - Draw data alignment in memory.
 - little endian, big endian
 - unsigned and signed integer
 - Convert 2's complement integer format among hexadecimal, decimal and binary.
 - BCD, ASCII, convert data to ASCII.
4. State segment registers and memory segmentation.
 - six internal segment register, 16-byte address boundary
5. Describe Instruction Pointer.
6. List general purpose data registers.
7. Describe pointer and index registers.
8. Describe flag register and typical flags.
9. State the generation of a real-mode memory address.
10. State the operation of stack.
11. Describe real-mode I/O address space.

3. Chapter 3. Assembly Language Programming Methodology

1. Describe the concept of software:
 - machine language, assembly language, high level languages, source code, assembler, compiler.
2. Describe the steps of assembly language program development.
 - describe, plan, code, assemble, run, verify
3. Describe the evolution of 8086 family instruction set.
4. Register operand addressing mode
5. Immediate operand addressing mode
6. 16-bit memory operand addressing mode (direct, register indirect, based, indexed)
7. 32-bit memory operand addressing mode

4. Chapter 4. Assembly Language Coding and Debugging

1. Convert assembly language instructions to machine code.
2. Use "DEBUG" program to debug.

5. Chapter 5. Real-mode 80386DX Programming I

1. Use data transfer instructions.
2. Use arithmetic instructions.
3. Use logic instructions.
4. Use shift instructions.
5. Use rotate instructions.
6. Use bit test and bit scan instructions.

6. Chapter 6. Real-mode 80386DX Programming II

1. Use flag-control instructions.
2. Use compare and set instructions.
3. Use jump instructions.
4. Use subroutine instructions.
5. Use loop instructions.
6. Use string instructions.

7. Chapter 7. Program Development with MS-MASM

1. Describe statement syntax.
2. State pseudo operations.

8. Chapter 8. Protected-mode Software Architecture of 80386DX

1. Protected-mode register model, new registers, extension of registers.
2. Global Descriptor Table Register (GDTR)
3. Interrupt Descriptor Table Register (IDTR)
4. Local Descriptor Table Register (LDTR)
5. Task Register (TR)
6. Control Register (CR), protected-mode enable/disable
7. Segment Selector Register (SSR)
8. Virtual address and virtual address space
9. Segmented partitioning of virtual address space
10. Physical address space and virtual-to-physical address translation.
11. Paged partitioning of virtual address space and vir-to-phy address translation
12. Descriptor and page table entries.
13. Protected-mode system-control instruction set
14. Protection model
15. Privilege level
16. Task switching

9. Chapter 9. Memory and I/O Interfaces of 80386DX Microprocessors

1. Memory/IO interface
2. Interrupt interface
3. DMA interface
4. Coprocessor interface
5. System clock
6. Nonpipelined and pipelined bus cycles
7. Read and write bus cycle timing
8. Hardware organization of memory address space.
9. Memory interface circuitry
 - address latches and buffers
 - data bus transceivers
 - address decoders
10. PLA
11. Isolated and memory-mapped I/O.

10. Chapter 10. Memory Devices, Circuits and Subsystem Design

1. Program and data-storage memory.
2. Read only memory (ROM)
 - PROM, EPROM
 - block diagram, read operation
3. Static RAM

- block diagram
 - read and write operations
4. Dynamic RAM
 5. FLASH memory
 6. Describe parity checking and related circuit.
 7. Cache memory, hit ratio, 82385DX cache controller.
 8. Organization and operation of direct mapped cache memory.
 9. Organization and operation of two-way associative cache memory.

11. Chapter 11. I/O Circuits and LSI Peripheral Devices

1. Core and special-purpose I/O.
2. 8-byte-wide parallel output circuit
3. Time-delay loop and blinking an LED
4. 8-byte-wide parallel input circuit
5. I/O handshaking and a parallel printer interface
6. 8255A programmable peripheral interface(PPI)
 - block diagram
 - control words
 - isolated I/O
 - memory mapped I/O
7. 82C54 programmable interval timer
 - diagram, architecture
 - examples
8. 82C37A programmable direct memory access (PDMA) controller
 - interface, internal architecture
 - examples

12. Chapter 12. Interrupt and Exception Processing of 80386DX

1. Types of interrupts and exceptions.
2. Interrupt vector and descriptor tables
3. Interrupt instructions
4. Disable and enable interrupts
5. External hardware-interrupt interface and sequence
6. 82C59A programmable interrupt controller
 - block diagram
 - programming the 8259A