16.317 Microprocessor I
Course Review

1. Microprocessors and Microcomputers - Chapter 1.
    a. Describe general architecture of a microcomputer system
    b. List recent Intel microprocessors, describe benchmarking
2. Real-Mode Software Architecture of the 80386DX Microprocessors - Chapter 2.
    a. Describe the internal architecture of 80386DX.
        • Six functional units of 80386
    b. Describe real-mode software architecture.
        • General-purpose registers, register size
        • Segment registers (CS, DS, ES, FS, GS, SS)
        • IP, SP, BP etc.
    c. Draw data alignment in memory.
        • Little-endian
        • Aligned/misaligned double word, word
        • Unsigned/signed integer number
    d. Convert 2's complement integer format among hexadecimal, decimal and binary.
    e. Describe segment registers and memory segmentation.
    f. Describe flag register and typical flags.
    g. State the generation of a real-mode memory address.
    h. State the operation of stack.
        • Stack growth direction, size of current stack
        • PUSH POP instructions
    i. Describe real-mode I/O address space.
3. Real-Mode Assembly Language Programming Methodology - Chapter 3.
    a. Describe the steps of assembly language program development.
    b. Describe the addressing modes of 80386DX.
        • Register operand addressing mode
        • Immediate operand addressing mode
        • 16-bit memory operand addressing mode (direct, register indirect, based, indexed)
4. Assembly Language Coding and Debugging - Chapter 4.
    a. Convert assembly language instructions to machine code.
    b. Use "DEBUG" program to debug.
5. Real-mode 80386DX Programming I - Chapter 5.
    a. Use data transfer instructions.
    b. Use arithmetic instructions.
    c. Use logic instructions.
    d. Use shift instructions.
    e. Use rotate instructions.
    f. Use bit test and bit scan instructions.
6. Real-mode 80386DX Programming II - Chapter 6.
    a. Use flag-control instructions.
    b. Use compare and set instructions.

      c. Use jump instructions.

      d. Use subroutine instructions.

7. Protected-mode Software Architecture of 80386DX - Chapter 8.

      a. Describe protected-mode register model.

- Fig 8.2, 8.4, 8.6, Example 8.7
- GDTR, LDTR, IDTR (base, limit)
- Control register

      b. Describe protected-mode memory management and address translation.

- Fig 8.14, Example 8.8
- Fig 8.19

      c. State multitasking and protection.

- Fig 8.37-38

8. Memory and I/O Interfaces of the 80386DX Microprocessors - Chapters 9.

      a. Figure 9.3 block diagram of 80386DX

- Signal description figure 9.4
- BE signals and data size
- Figure 9.7 bus-cycle indication signals

      b. Describe system clock and bus cycles. (Fig 9.10-17)

- System clock, MPU clock
- Non-pipelined vs. pipelined bus cycle

      c. Construct hardware organization of memory address space.

- Fig 9.20-24
- Fig 9.25 memory interface
- Fig 9.39 PLA
- Fig 9.51 byte-wide I/O interface block diagram

      d. I/O instructions

      e. DMA

9. Memory Devices, Circuits and Subsystem Design - Chapter 10.

      a. ROM, SRAM, DRAM

      b. Describe parity checking and related circuit. (Fig 10.24)

      c. Memory system design using memory IC devices (Fig 10.39)

10. I/O Circuits - Chapter 11.

      a. Compare memory mapped I/O and isolated I/O

11. PIC microcontroller

      a. Harvard vs Von Neumann architecture

      b. Data memory organization, banks, Special Function Registers (STATUS), General Function Registers, W register

      c. Direct addressing and indirect addressing (FSR, INDF)

      d. Instruction Set: bit (bsf, bcf), byte (e.g. movlw, movf, addwf, subwf), conditional branch (e.g. btfsc, btfss incfsz, decfsz), goto

      e. Input/Output using PIC: TRISA, PORTA etc.