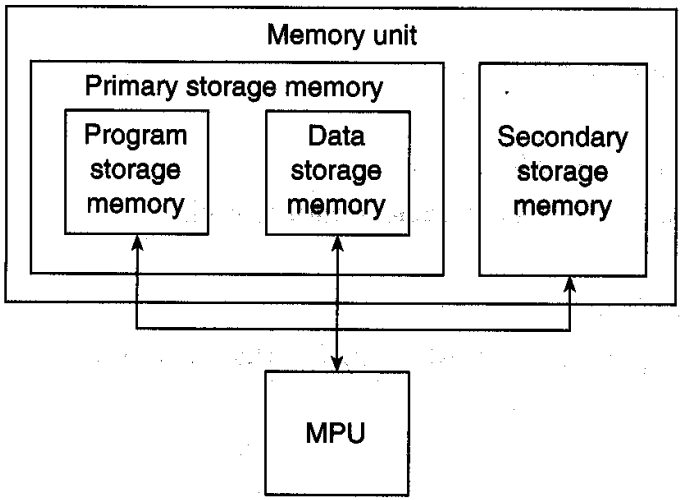
Chapter 9

Memory Devices, Circuits, and Subsystem Design

Introduction

9.1 Program and Data Storage Memory—✓
9.2 Read-Only Memory—✓
9.3 Random Access Read/Write Memories—✓
9.4 Parity, Parity Bit, and Parity-Checker/Generator Circuit
9.5 FLASH Memory
9.6 Wait-State Circuitry—✓
9.7 8088/8086 Microcomputer System Memory Interface Circuitry—✓

9.1 Program and Data Storage Memory– The Memory Unit

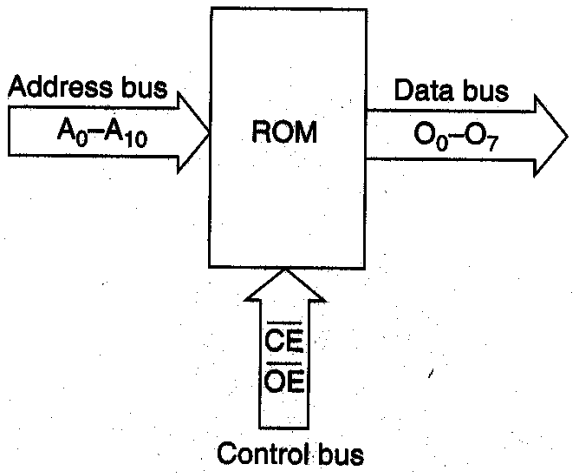


- Memory—provides the ability to store and retrieve digital information
  - Instructions of a program
  - Data to be processed
  - Results produced by processing
- Organization of the Microcomputer memory unit
  - Secondary storage—stores information that is not currently in use
    - Slow-speed
    - Very large storage capacity
    - Implemented with magnetic/optical storage devices—in PC
      - Hard disk drive
      - Floppy disk drive
      - Zip drive
  - Primary storage—stores programs and data that are currently active
    - High-speed
    - Smaller storage capacity
    - Implemented with semiconductor memory
  - Partitioning of Primary Storage
    - Program storage memory—holds instructions of the program and constant information such as look-up tables
      - EPROM (BIOS in PC)
      - FLASH memory
      - DRAM (volatile code storage in a PC)
    - Data storage memory—holds data that frequently changes such as the information to be processed by a program
      - SRAM
      - DRAM (PC)

9.2 Read-Only Memory– Types

- Read-only memory (ROM)
  - Used for storage of machine code of program
  - Stored information can only be read by the MPU
  - Information is nonvolatile—not lost when power turned off
  - Types:
    - ROM—mask-programmable read only memory
      - Programmed as part of manufacturing process
      - Lowest cost
      - High volume applications
    - PROM—one-time programmable read-only memory
      - Permanently programmed with a programming instrument
    - EPROM—erasable programmable read-only memory
      - Programmed like a PROM
      - Erasable by Ultraviolet light
  - Electrically alterable ROM-like devices
    - FLASH memory
    - EEROM (E^2ROM)

9.2 Read-Only Memory– Block Diagram



- Block diagram of the ROM, PROM, and EPROM are essentially the same
- Signal interfaces
  - Address bus (A10-A0)—MPU inputs address information that selects the storage location to be accessed
  - Data Bus (D7-D0)—information from the accessed storage location output to be read by MPU
  - Control bus—enables device and/or enables output from device
    - CE* = chip enable—active 0; 1 low-power stand by mode
    - OE* = output enable—active 0; 1 high-Z state
- Byte capacity– number of bytes a device can store
  - Calculated from number of address bits

    EX: Address = 11-bit address

    Storage capacity = 2^{11} = 2048 bytes
- Organization—how the size of a ROM is described
  - Formed from capacity and data bus width

    EX: 2048 X 8 or just 2K X 8
- Storage density—number of bits of storage in a ROM
  - Calculated from byte capacity and data width

    EX: Storage density = 2048 X 8 = 16384 bits (16K bits)

9.2 Read-Only Memory– Organization and Capacity

- Example:

  A ROM device has 15 address lines and 8 data lines. What are the address range, byte capacity, organization, and storage density?

- Solution:
  - Address range

    A14-A0 = 000 0000 0000 0000_2 → 111 1111 1111 1111_2

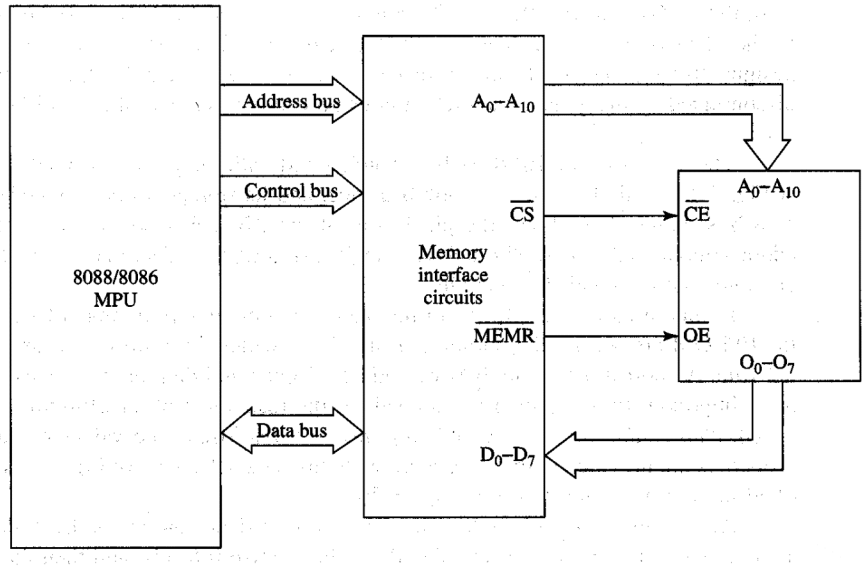
    = 0000H → 7FFFH
  - Byte capacity

    2^{15} = 32,768 bytes = 32K bytes
  - Organization

    32768 X 8 bit
  - Storage density

    32768 x 8 = 262144 bits = 256K bits

9.2 Read-Only Memory– Operation



- Read operation
  - MPU outputs address and control information on its bus.
  - Interface circuit applies Address A10-A0 to the address inputs of the ROM to select a specific byte wide storage location
  - Interface circuits decode additional address bits to produce a chip select output
  - Logic 0 at CS* applied to the CE* input of the ROM to enable it for operation
  - Memory interface circuitry produces appropriately timed MEMR* output
  - MEMR* applied to OE* input of the ROM to enable the information at the addressed storage location onto the output bus D7-D0
  - Memory interface supplies the byte of data from the ROM to the MPUs data bus
  - MPU reads the byte of data from the ROM from its data bus

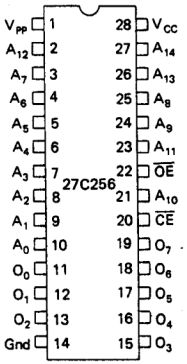
9.2 Read-Only Memory– Standard EPROM ICs

EPROM	Density (bits)	Capacity (bytes)
2716	16K	2K × 8
2732	32K	4K × 8
27C64	64K	8K × 8
27C128	128K	16K × 8
27C256	256K	32K × 8
27C512	512K	64K × 8
27C010	1M	128K × 8
27C020	2M	256K × 8
27C040	4M	512K × 8

- EPROM part numbers formed by adding the prefix "27" to the device total Kbytes of storage capacity
  - Examples:
    - 16K bit EPROM → 2716
    - 32K bit EPROM → 2732
    - 1M bit EPROM → 27C010
- Most EPROM available in byte wide organization
  - Examples:
    - 2764 → 8K X 8
    - 27C020 → 256K X8
- NMOS versus CMOS process
  - Manufacturing processes used to make EPROMs
    - NMOS=N-channel metal-oxide semiconductor
    - CMOS= complementary symmetry metal-oxide semiconductor
    - "CMOS" designated by "C" in part number
  - NMOS—older devices such as 2716 and 2732
  - CMOS—all newer devices 27C64 and up

9.2 Read-Only Memory– Pin Layouts

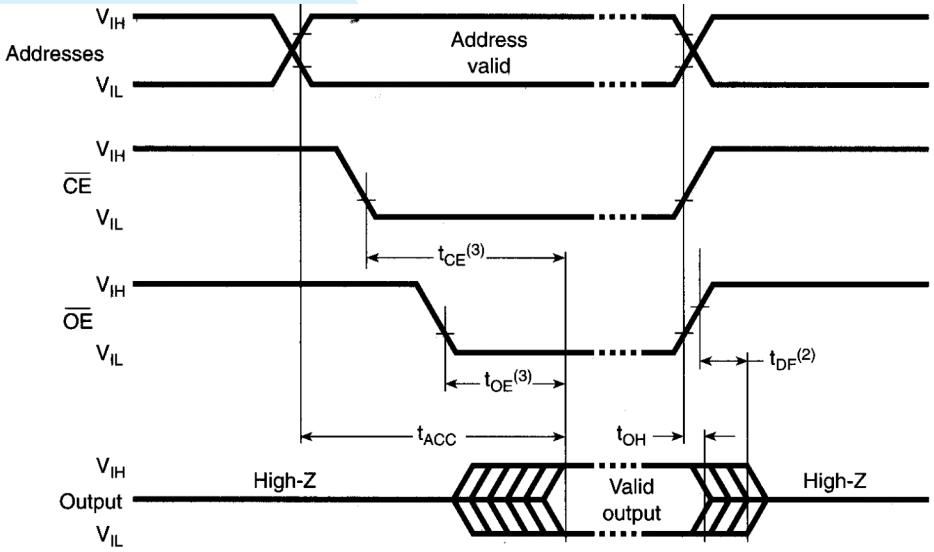
27C512	27C128	27C64	2732A	2716	Pin
A_{15}	V_{PP}	V_{PP}			1
A_{12}	A_{12}	A_{12}			2
A_7	A_7	A_7	A_7	A_7	3
A_6	A_6	A_6	A_6	A_6	4
A_5	A_5	A_5	A_5	A_5	5
A_4	A_4	A_4	A_4	A_4	6
A_3	A_3	A_3	A_3	A_3	7
A_2	A_2	A_2	A_2	A_2	8
A_1	A_1	A_1	A_1	A_1	9
A_0	A_0	A_0	A_0	A_0	10
O_0	O_0	O_0	O_0	O_0	11
O_1	O_1	O_1	O_1	O_1	12
O_2	O_2	O_2	O_2	O_2	13
Gnd	Gnd	Gnd	Gnd	Gnd	14



Pin	2716	2732A	27C64	27C128	27C512
28			V_{CC} / $\overline{PGM}$	V_{CC} / $\overline{PGM}$	V_{CC}
27			N.C.	A_{13}	A_{14}
26	V_{CC}	V_{CC}	A_8	A_8	A_{13}
25	A_8	A_8	A_9	A_9	A_8
24	A_9	A_9	A_{11}	A_{11}	A_9
23	V_{PP}	A_{11}	$\overline{OE}$	$\overline{OE}$	A_{11}
22	$\overline{OE}$	$\overline{OE}/V_{PP}$	A_{10}	A_{10}	$\overline{OE}/V_{PP}$
21	A_{10}	A_{10}	$\overline{CE}$	$\overline{CE}$	A_{10}
20	$\overline{CE}$	$\overline{CE}$	O_7	O_7	$\overline{CE}$
19	O_7	O_7	O_6	O_6	O_7
18	O_6	O_6	O_5	O_5	O_6
17	O_5	O_5	O_4	O_4	O_5
16	O_4	O_4	O_3	O_3	O_4
15	O_3	O_3			O_3

- EPROM pin layouts are designed for compatibility
  - Permit easy upgrade from lower to higher density
  - Publish pin layouts of future densities
  - Allows design of circuit boards to support drop in upgrade to higher densities
- Most pins are independent and serve a common function for all densities
  - Examples:
    - pin 10– A0
    - pin 11--O0
    - pin 14– Gnd
- Some have one multi-function pin
  - OE*/Vpp
  - Vpp mode during programming only

9.2 Read-Only Memory– EPROM Switching Waveforms



- Timing of the read operation
  - Output data is not immediately available at the outputs
    - Delays exist between the application of the address,CE* and OE* signals and the occurrence of a valid output
    - tacc= access time—address to valid output delay time
    - tCE= chip-enable time—chip enable to valid output delay
    - tOE=output-enable time—output enable to valid data delay
  - To assure that the MPU reads valid data, these inputs must be applied at the appropriate times
    - Responsibility of the memory interface circuitry
  - Another delay occurs at the removal of OE* before the outputs lines are returned to the high-Z state
    - tDF= chip-deselect time—time for the outputs to recover

9.2 Read-Only Memory– 27C256 Read Cycle Timing Characteristics

Versions	$V_{CC} \pm 5\%$	27C256-120V05		27C256-135V05		27C256-150V05		27C256-1 P27C256-1 N27C256-1		27C256-2 P27C256-2 N27C256-2		27C256 P27C256 N27C256		Unit
	$V_{CC} \pm 10\%$			27C256-135V10		27C256-150V10				27C256-20 P27C256-20 N27C256-20		27C256-25 P27C256-25 N27C256-25		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{ACC}	Address to output delay		120		135		150		170		200		250	ns
t_{CE}	$\overline{CE}$ to output delay		120		135		150		170		200		250	ns
t_{OE}	$\overline{OE}$ to output delay		60		65		70		75		75		100	ns
t_{DF}(2)	$\overline{OE}$ high to output high-Z		30		35		45		55		55		60	ns
t_{OH}(2)	Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change—whichever is first	0		0		0		0		0		0		ns

Notes:
1. A.C. characteristics tested at V_{IH} = 2.4 V and V_{IL} = 0.45 V.
   Timing measurements made at V_{OL} = 0.8 V and V_{OH} = 2.0 V.
2. Guaranteed and sampled.
3. Package Prefixes: No Prefix = CERDIP; N = PLCC; P = Plastic DIP.

- EPROM part numbers include access time and power supply tolerance information
  - 27C256120V05
    - tACC = 120ns
    - Vcc = ± 5%
  - 27C256-1
    - tACC = 170ns
    - Vcc = ± 10% (standard—unmarked)
- Maximum access times of the 27C256-120V05
  - tacc=120ns
  - tCE= 120ns
  - tOE= 60ns
  - tDF= 30ns
  - Note that tacc and tCE should be applied at the same time
    - More delays in tCE path!

9.2 Read-Only Memory– DC Electrical Characteristics

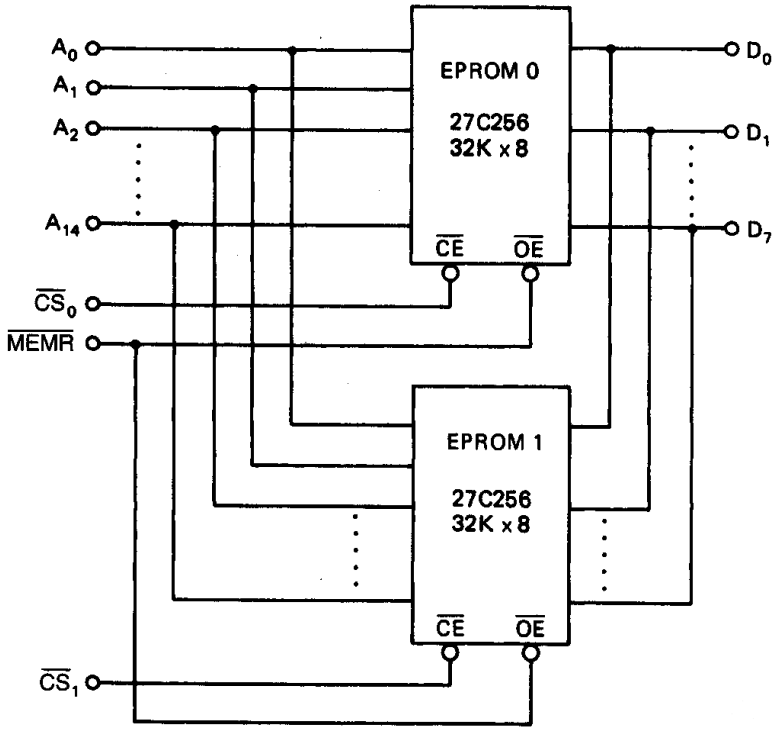
Symbol	Parameter		Notes	Min	Typ(3)	Max	Unit	Test Conditions
I_{LI}	Input load current				0.01	1.0	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output leakage current					± 10	µA	V_{OUT} = 0V to V_{CC}
I_{PP_1}	V_{PP} read current		5			200	µA	V_{PP} = V_{CC}
I_{SB_1}	V_{CC} current standby	TTL	8			1.0	mA	$\overline{CE}$ = V_{IH}
I_{SB_2}		CMOS	4			100	µA	$\overline{CE}$ = V_{CC}
I_{CC_1}	V_{CC} current active		5, 8			30	mA	$\overline{CE}$ = V_{IL} f = 5 MHz
V_{IL}	Input low voltage (± 10% supply) (TTL)			–0.5		0.8	V	
	Input low voltage (CMOS)			–0.2		0.8		
V_{IH}	Input high voltage (± 10% supply) (TTL)			2.0		V_{CC} + 0.5	V	
	Input high voltage (CMOS)			0.7 V_{CC}		V_{CC} + 0.2		
V_{OL}	Output low voltage					0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output high voltage			3.5			V	I_{OH} = –2.5 mA
I_{OS}	Output short circuit current		6			100	mA	
V_{PP}	V_{PP} read voltage		7	V_{CC} – 0.7		V_{CC}	V	

Notes:

1. Minimum D.C. input voltage is –0.5V. During transitions, the inputs may undershoot to –2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
3. Typical limits are at V_{CC} = 5V, T_A = +25°C.
4. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
5. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with outputs O_0 to O_7 unloaded.
6. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
7. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
8. V_{IL}, V_{IH} levels at TTL inputs.

- Some important operating DC voltage and current ratings
  - Vcc is ±5% or ± 10%
  - High and low output voltages
    - V_{OL} max = 0.45V
    - V_{OH} min = 3.5V
  - High and low input voltages
    - V_{IL} max = .8V (TTL)
    - V_{IH} min = 2V (TTL)
  - V_{cc} current—active
    - I_{cc1} = 30 ma (TTL)
  - V_{cc} current—standby
    - I_{ss1} = 1 ma (TTL)

9.2 Read-Only Memory– Expanding Byte Capacity



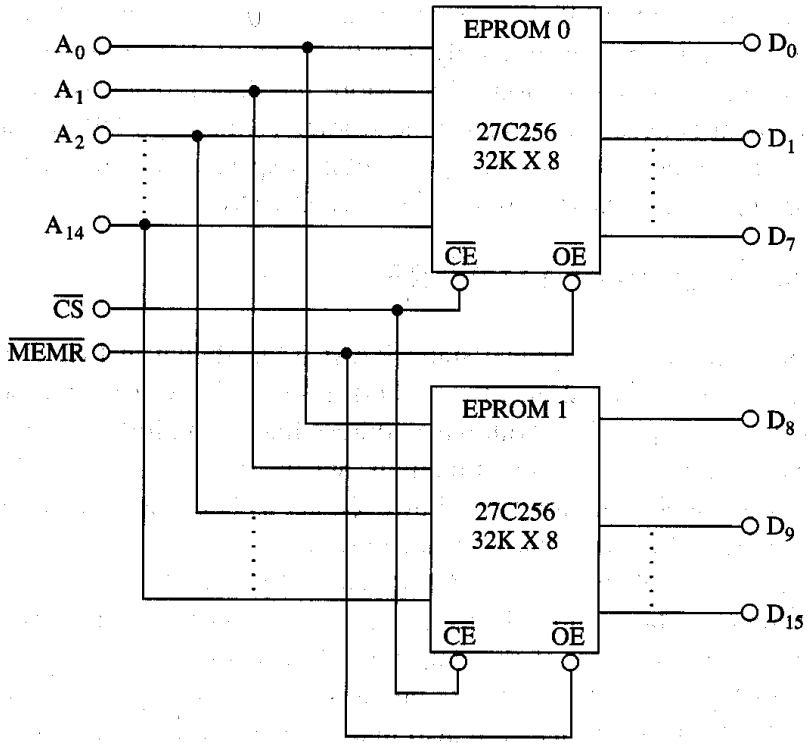
- Many applications require more ROM capacity than is available in a single device
  - Need more bytes of storage
  - Connects to a wider data bus
- Expanding byte capacity with 2 EPROMS
  - Connect address bus lines in parallel
  - Connect output lines in parallel
  - Connect OE* in parallel
  - Enable chips with separate chip selects
    - Address bit A15 decoded to produce CS0* and CS1*
      - A15=0 → CS0*
      - A15=1 → CS1*
      - Implemented with inverting buffer
  - Byte capacity

    2^{16} = 64K bytes
  - Organization

    64K X 8 bit
  - Storage density

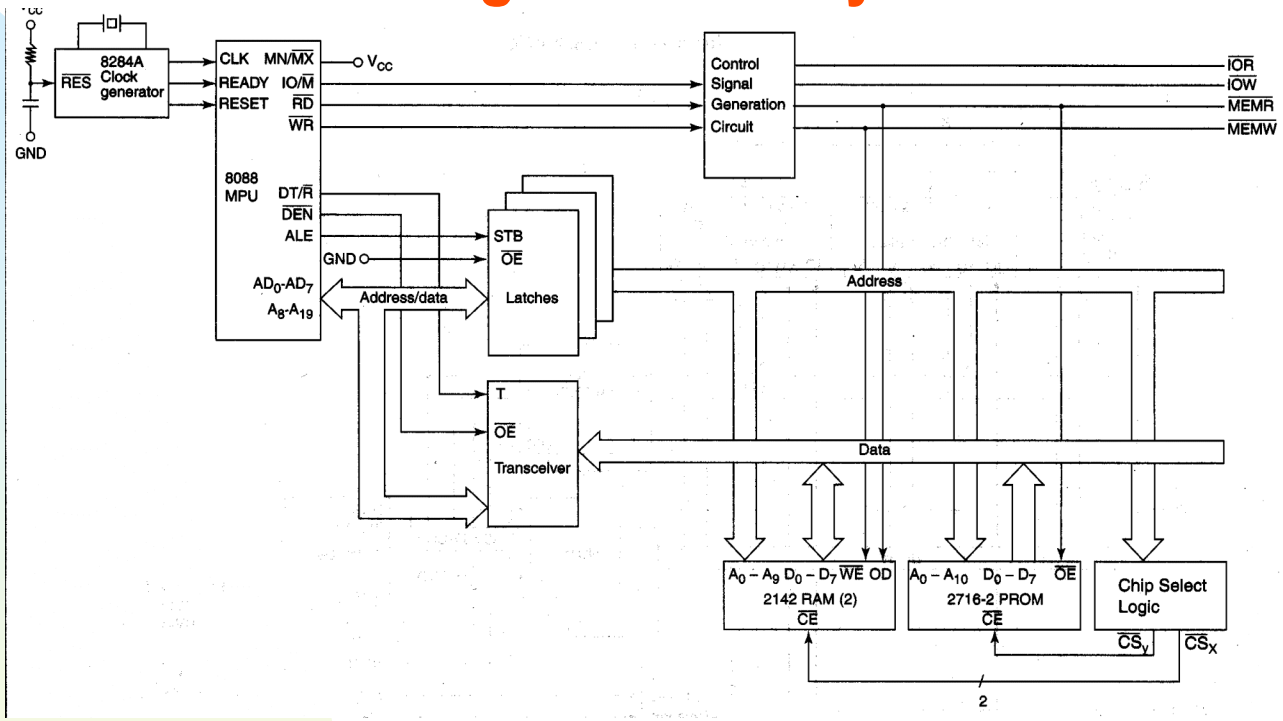
    2 X 32K x 8 = 512K bits

9.2 Read-Only Memory– Expanding Word Length



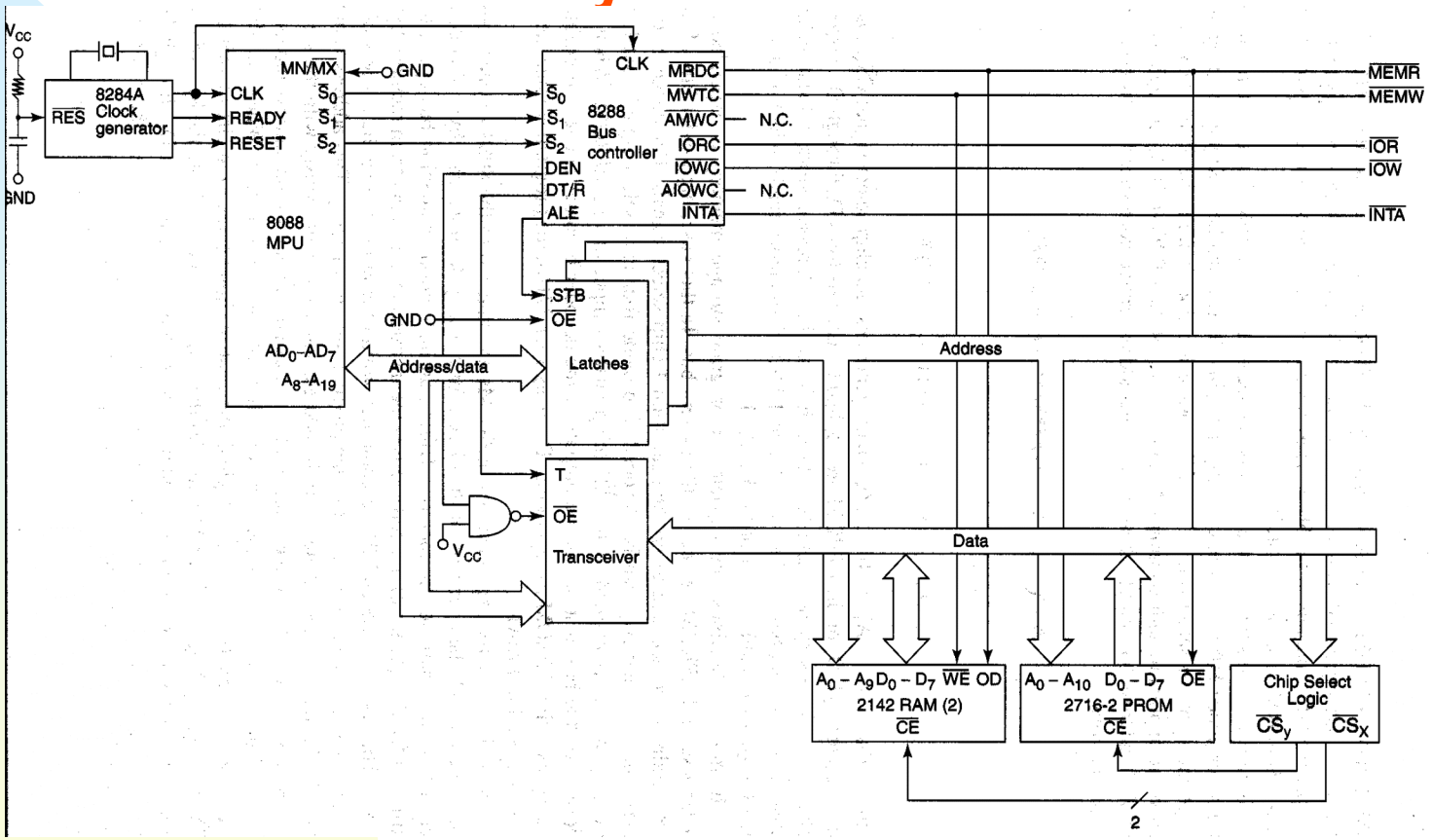
- Expanding word length with 2 EPROM
  - Connecting to 8086 16-bit data bus
    - Connect address bus lines in parallel
    - Connect CE* in parallel
    - Connect OE* in parallel
    - 8 data outputs of EPROM 0 used to supply the lower data bus lines D0-D7
    - 8 data outputs of EPROM 1 used to supply the upper 8 data bus lines D8-D15
  - Byte capacity
    $2 \times 2^{15} = 64K$ byte
  - Organization
    32K X 16 bit
  - Storage density
    32K x 16 = 512K bits

9.7 8088/8086 Microcomputer System Memory Circuitry– Minimum-Mode 8088 System Program Memory Interface*



- Program memory
  - Implemented with a single 2716 EPROM—2K X 8-bit
  - Program memory address range
    A10-A0 = 00000H – 007FFH
  - CS_Y* =0 produced by decoding additional address bit
    ie. A11-A19 = 0 → CS_Y*
    A11-A19 = 100000000 → CS_X*
  - MEMR* → OE*

9.7 8088/8086 Microcomputer System Memory Circuitry– Maximum-Mode 8088 System Memory Interface*

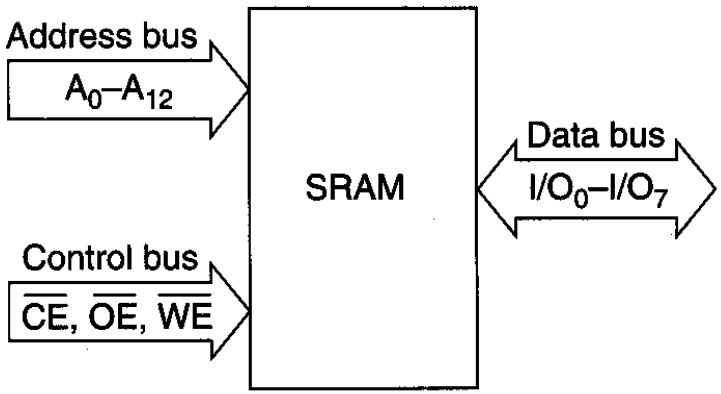


- Enable signals for address latches, data bus transceivers, RAM, and PROM produced by bus controller

9.3 Random Access Read/Write Memories– Types of RAMs

- Random Access Read/Write Memory (RAM)
  - Used for temporary storage of data and program information
  - Stored information can be altered by MPU—read or written
    - Information read from RAM
    - Modified by processing
    - Written back to RAM for reuse at a later time
  - Information normally more frequently randomly accessed than ROM
  - Information is volatile— lost when power turns off
  - Types:
    - Static RAM (SRAM)— data once entered remains valid as long as power supply is not turned off
      - Lower densities
      - Higher cost
      - Higher speeds
    - DRAM—data once entered requires both the power to be maintained and a periodic refresh
      - Higher densities
      - Lower cost
      - Lower speeds
      - Refresh requires additional circuitry

9.3 Random Access Read/Write Memories–
SRAM Block Diagram



- Signal interfaces
  - Address bus (A12-A0)—MPU inputs address information that selects the storage location to be accessed
  - Data Bus (I/O7-I/O0)—input/output of information for the accessed storage location from/to MPU
  - Control bus—enables device, enables output from device, and selects read/write operation
    - CE* = chip enable—active 0
    - OE* = output enable—active 0
    - WE* = write enable

      0 = write to RAM

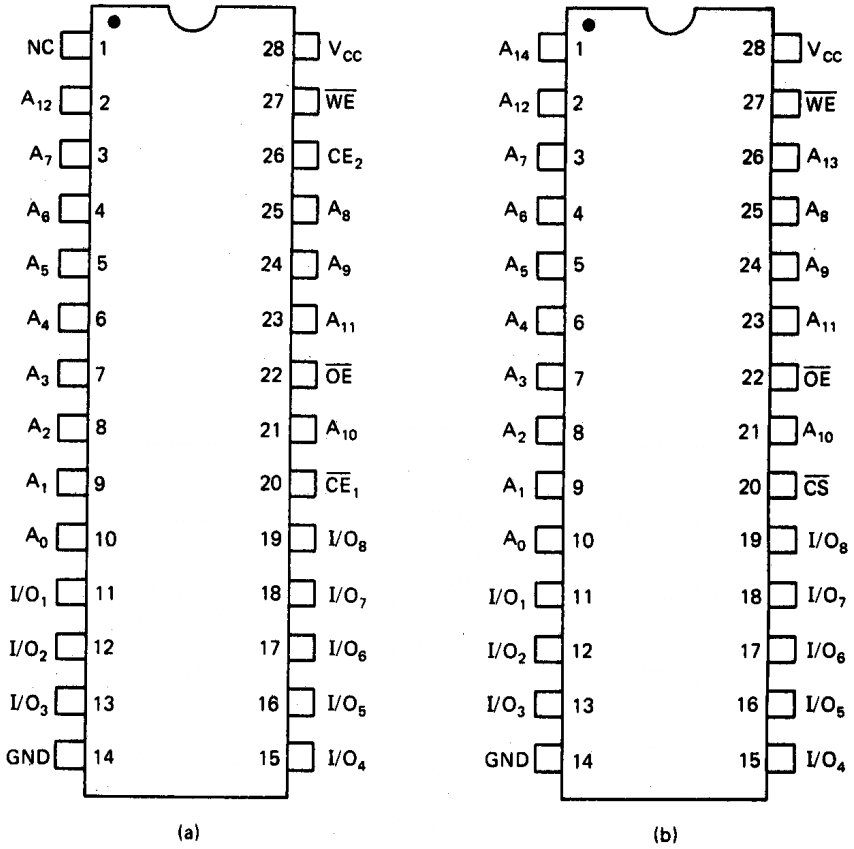
      1 = read from RAM

9.3 Random Access Read/Write Memories– Standard SRAM ICs

SRAM	Density (bits)	Organization
4361	64K	64K × 1
4363	64K	16K × 4
4364	64K	8K × 8
43254	256K	64K × 4
43256A	256K	32K × 8
431000A	1M	128K × 8

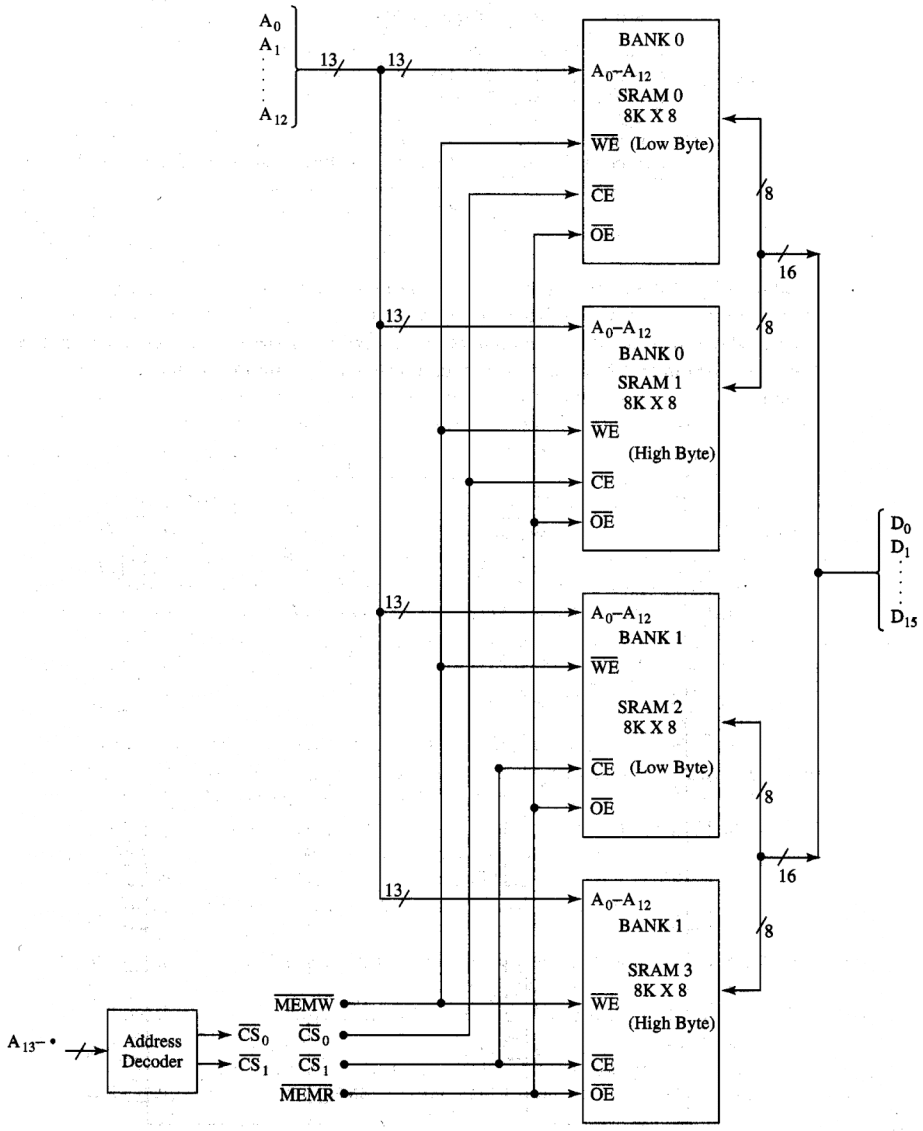
- Part numbers vary widely by manufacturer—Hitachi/NEC use “43xxx
- SRAMs are available in a variety of densities and organization
  - Typical SRAM densities
    - 64K bit
    - 256K bit
    - 1M bit
  - Typical organizations of the 64K bit SRAM
    - 64K X 1 bit
    - 16K X 4 bit
    - 8K X 8 bit

9.3 Random Access Read/Write Memories– Pin Layout of SRAMs



- 4364 and 43256A pin layouts are designed for compatibility
- 4364 pin configuration (Fig a)
  - A12-A0 → 13-bit address
    2^{13} = 8K bytes
  - I/O7-I/O0 → byte wide
  - Pin 1 NC = no connect
  - Pin 27 WE*
  - Pin 20 CE1* → active 0
  - Pin 26 CE2 → active 1
  - Pin 22 → OE*
  - Pin 28 Vcc
  - Pin 14 GND
- 43256A differences (Fig b)
  - Pin 1 → A14
  - Pin 26 → A13
  - Pin 20 called CS* (function unchanged)

9.3 Random Access Read/Write Memories– Expanding Word-Width and Capacity



- Most SRAM subsystems
  - Require both word-width and bit capacity expansion
  - Require the ability to write on byte-wide or word wide basis– design only supports words
- Expansions performed in a similar way as for EPROMs
- 16K X 16-bit SRAM circuit
  - A0-A12 in parallel
  - A13 decoded to form CS0* and CS1*
    - CS0* → enable Bank 0
    - CS1* → enable Bank 1
  - SRAMs 0 & 2—input/outputs connected in parallel and supply low byte of data bus
  - SRAMs 1 & 3—input/ outputs connected in parallel and supply high byte of data bus
  - MEMW* and MEMR* produces independent write and read enables

MEMW*	MEMR*	Data Transfer
0	0	Invalid
0	1	Word write
1	0	Word read
1	1	Inactive

  - **How can the circuit be modified to support byte wide write?**

9.3 Random Access Read/Write Memories– Standard Read/Write Cycle Times

Part number	Read/write cycle time
4364-10	100 ns
4364-12	120 ns
4364-15	150 ns
4364-20	200 ns

- Speed of a SRAM identified as read/write cycle time
  - Variety of speeds available—4364 available in speeds ranging from 100ns to 200ns
  - Shorter the cycle time the better
- Designated by a dash speed indicator following the part number

  -10 = 100ns

  -12 = 120ns

9.3 Random Access Read/Write Memories– DC Electrical Characteristics

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}			1	µA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}			1	µA	$V_{I/O}$ = 0 V to V_{CC} $\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}			(1)	mA	$\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O}$ = 0, Min cycle
	I_{CCA2}		5	10	mA	$\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O}$ = 0, DC current
	I_{CCA3}		3	5	mA	$\overline{CE}_1 \le 0.2$ V, $CE_2 \ge V_{CC} - 0.2$ V, $V_{IL} \le 0.2$ V, $V_{IH} \ge V_{CC} - 0.2$ V, f = 1 MHz, $I_{I/O}$ = 0
Standby supply current	I_{SB}			(2)	mA	$\overline{CE}_1 \ge V_{IH}$ or $CE_2 = V_{IL}$
	I_{SB1}			(3)	mA	$\overline{CE}_1 \ge V_{CC}-0.2$ V $CE_2 \ge V_{CC}-0.2$ V
	I_{SB2}			(3)	mA	$CE_2 \le 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –1.0 mA

Notes:

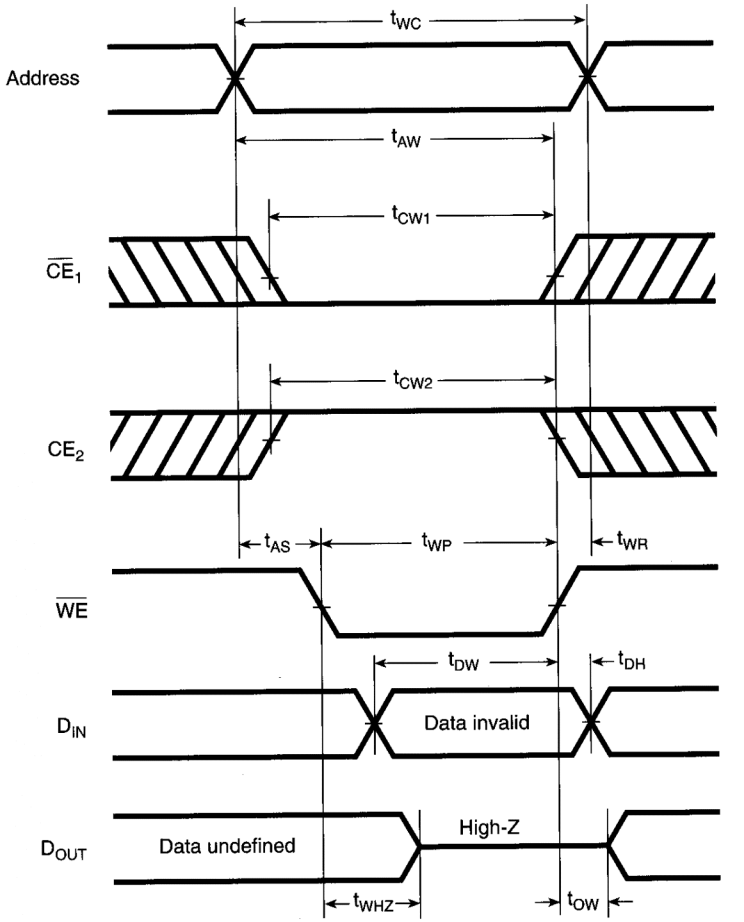
(1) µPD4364-10/10L: 45 mA max
µPD4364-12/12L/12LL: 40 mA max
µPD4364-15/15L/15LL: 40 mA max
µPD4364-20/20L/20LL: 35 mA max

(2) µPD4364-xx: 5 mA max
µPD4364-xxL: 3 mA max
µPD4364-xxLL: 3 mA max

(3) µPD4364-xx: 2 mA max
µPD4364-xxL: 100 µA max
µPD4364-xxLL: 50 µA max

- Some important operating DC voltage and current ratings
  - Vcc = 5V±10%
  - High and low output voltages
    - V_{OL} max = 0.4V
    - V_{OH} min = 2.4V
  - Icc—operating current
    - Varies based on frequency of repeated read/write cycles
    - I_{CCA1}—repeatedly performing fastest R/W cycle
      - I_{CCA1} max = 45mA @ -100ns
      - I_{CCA1} max = 35mA @ -200ns
    - I_{CCA1} increases with frequency
      - Fastest read cycle of –20 is ½ the frequency of the fastest –10 cycle
    - ICCA2—no R/W taking place (DC)
      - I_{CCA2} max = 10mA

9.3 Random Access Read/Write Memories– Write Cycle and Timing



Notes:
1. A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{W}$
2. $\overline{CE}_1$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transaction.
3. If $\overline{OE}$ is high the I/O pins remain in a high-impedance state.

- Timing is referenced to valid address
  - t_{WC} = write cycle time—address must remain valid for this period

    4364-10 t_{WC} = 100ns
  - Other important timing characteristics
    - t_{CW1} = CE1* to end of write time—minimum amount of time between CE1* becoming active and completion of write cycle

      4364-10 t_{CW1} = 80ns
    - t_{CW2} = CE2 to end of write time—minimum amount of time between CE2 becoming active and completion of write cycle

      4364-10 t_{CW2} = 80ns
    - t_{AS} = address set-up time—minimum amount of time the address must be stable before WE* becomes active

      4364-10 t_{AS} = 0ns
    - t_{WP} = write pulse width—minimum duration of the write

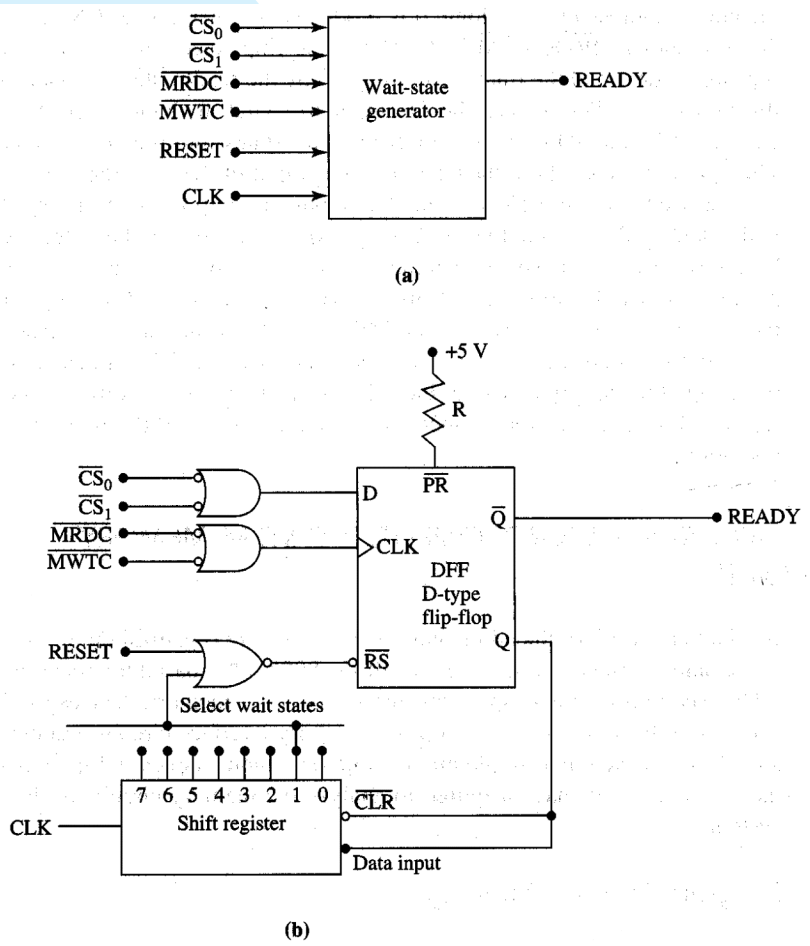
      4364-10 t_{WP} = 60ns
    - t_{DW} = data valid to end of write pulse—minimum time that input data must be maintained valid after the leading edge of WE*

      4364-10 t_{DW} = 60ns
    - t_{DH} = data hold time—minimum time that input data must be maintained valid after the training edge of WE*

      4364-10 t_{DH} = 0ns
    - t_{WR} = write recovery hold time—minimum time that must elapse from training edge of WE*before another write can be initiated

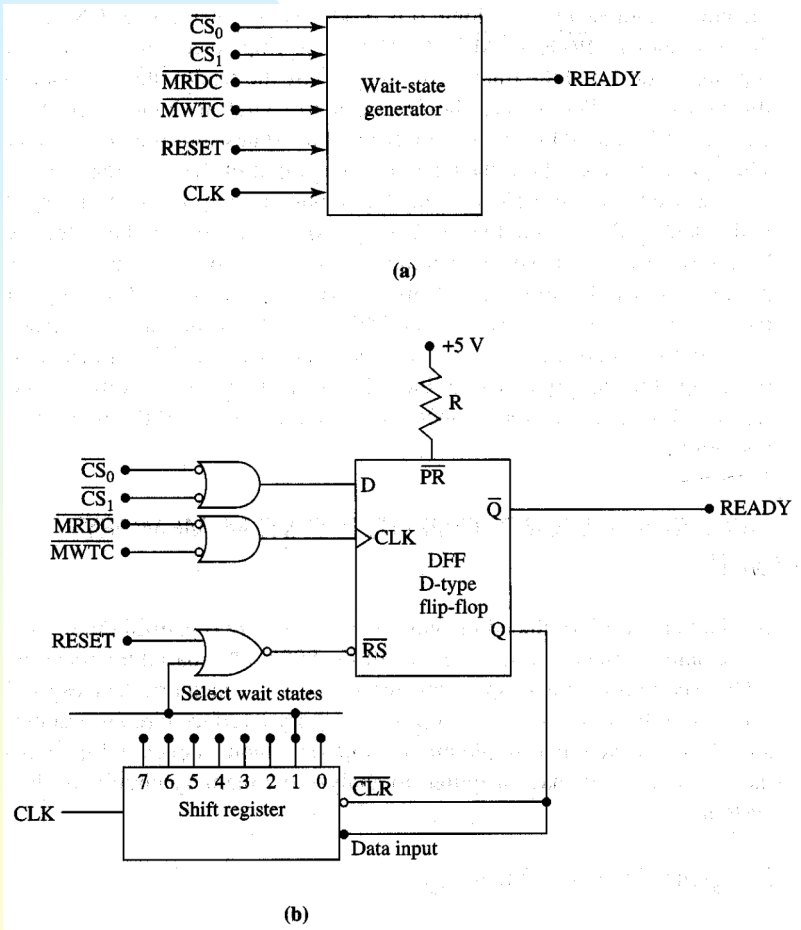
      4364-10 t_{WR} = 5ns

9.6 Wait-State Circuitry– Extending the Bus Cycle



- If the memory or I/O device is slow for the bus cycle of the MPU, read/write access cycles must be extended with wait states
  - Recall—bus cycle duration
    - 5MHZ 8088/8086 = 800ns
    - 8MHz 8088/8086 = 500ns
    - 10MHz 8086 = 400ns
  - Memory device speed not a problem with these older processor
    - 100MHz 80486—10ns clock
    - 2 clocks/bus cycle—20ns bus cycle duration
  - Slow I/O devices are a potential problem
  - Solution is wait-state generator circuit
    - Accepts CLK and bus cycle control signals as inputs
    - Circuit detects when bus cycle is in progress and delays active READY for an appropriate number of clock cycles

9.6 Wait-State Circuitry– Wait-State Generator Circuit Inputs and Outputs

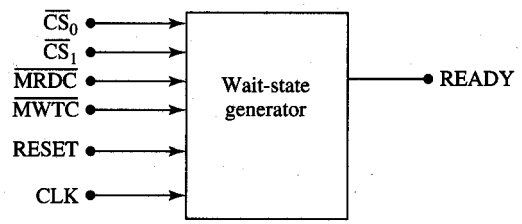


- Input of FF
  - CS0* and CS1* represents chip selects for the program and data storage memory
  - MRDC* and MWTC* correspond to read or write commands that occur during a memory access cycle
  - RESET is hardware reset of the MPU
  - Strapped output of the shift register is another input
  - CLK is MPU clock and drives shift register
- Output of FF
  - Q* output goes to the READY input of the MPU

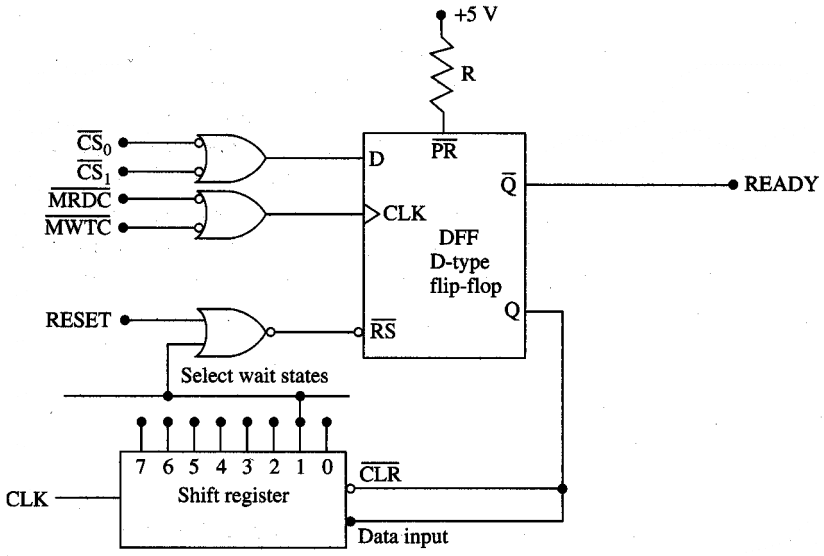
    0 = extend the bus cycle with wait states

    1= complete the current bus cycle

9.6 Wait-State Circuitry– Wait-State Generator Circuit Operation



(a)



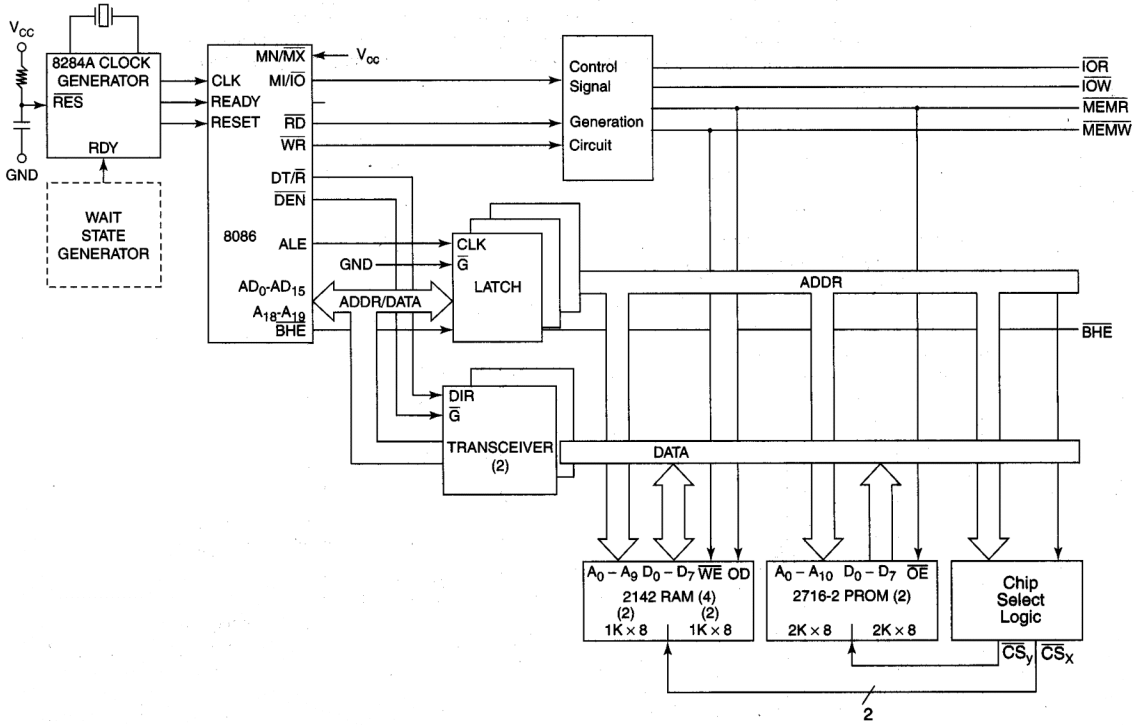
(b)

- Operation
  - Initial state after pulse at RESET is FF reset
    - Q* = 1 → READY
    - Q → CLR of shift register and makes SR outputs = 0
  - Bus cycle initiated
    - CS0* or CS1* becomes active = 0 making D=1
    - Pulse to 0 at either MRDC* or MWTC* clocks FF
    - FF sets making Q* = 0 and Q =1
      - Q* = 0 → READY inactive insert wait sates
      - Q = 1 applied as data input of SR
    - SR no longer held in clear state
    - CLK shifts logic 1 applied at Data input up through the SR
  - Bus cycle completes
    - When selected SR output (1) become 1, RS* input of FF made 0 and it resets

      Q = 0 → clears SR

      Q* = 1 → READY active and bus cycle completes
  - Bus cycle extended by how many clocks?

9.7 8088/8086 Microcomputer System Memory Circuitry– Minimum-Mode 8086 System Data Memory Interface

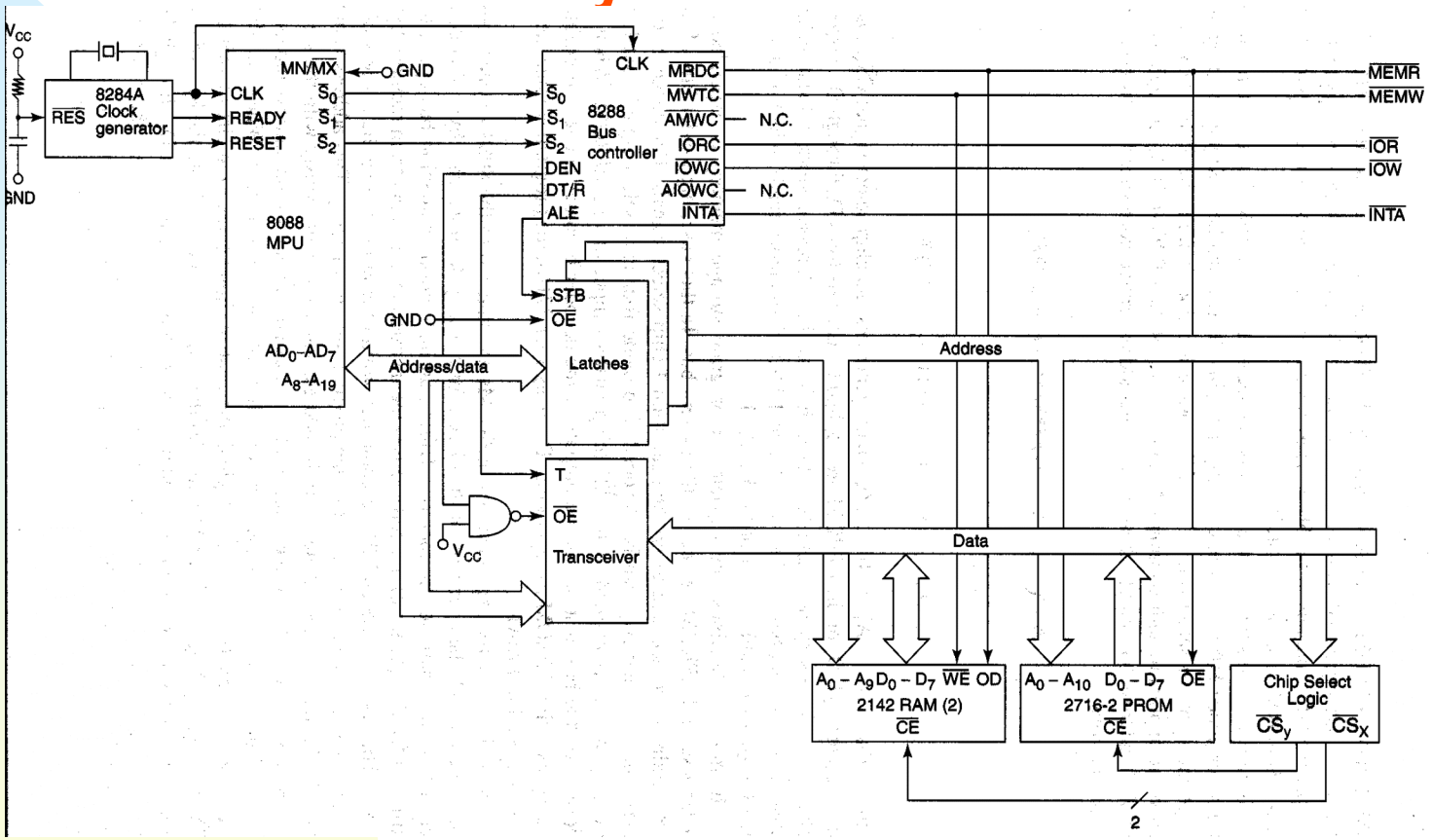


- Data memory
  - Implemented with 4 2142 1K X 4-bit SRAMs—1K X 16-bit
  - Assume: A11-A19 = 100000000 → CS_X*
  - SRAM memory address range

    A11-A0 = $1000\ 0000\ 0000_2$ – $1011\ 1111\ 1111_2$

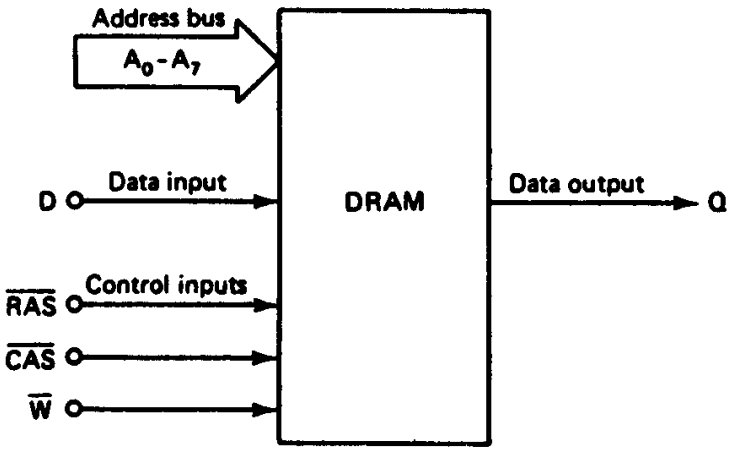
    = 00800H - 00BFFH
  - MEMW* → WE*
  - MEMR* → OD

9.7 8088/8086 Microcomputer System Memory Circuitry– Maximum-Mode 8088 System Memory Interface



- Enable signals for address latches, data bus transceivers, RAM, and PROM produced by bus controller

9.3 Random Access Read/Write Memories–
DRAM Block Diagram



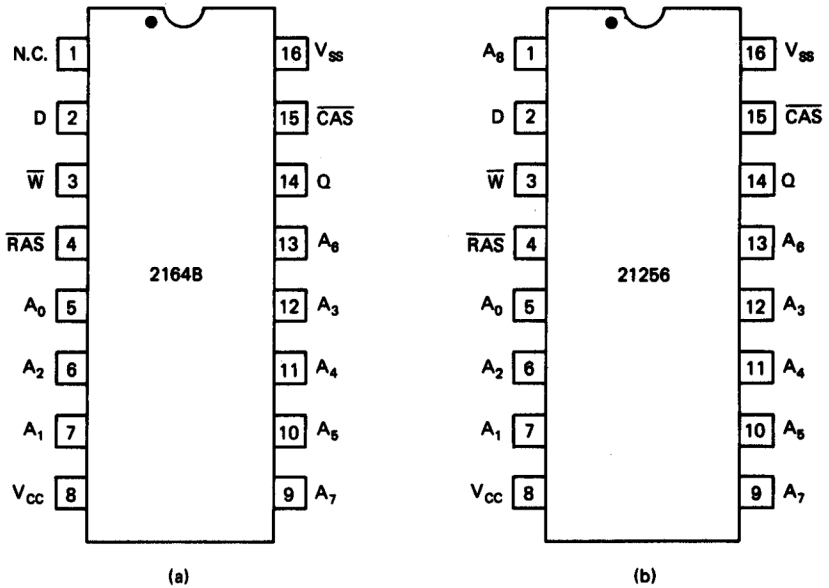
- DRAM signal interfaces
  - Address multiplexed in external circuitry into a separate row and column address
    - Row address = A_7-A_0
    - Column address = A_{15}-A_8
  - Special RAS* and CAS* inputs used to strobe address into DRAM
  - Row and column addresses applied at different times to address inputs A_0 through A_7
    - Row address first
    - Column address second
    - Known as “RAS before CAS”
    - Address reassembled into 16-bit address inside DRAM
  - Frequently data organizations are X1, X2, and X4
    - Separate data inputs and outputs
    - Data input labeled D
    - Data output labeled Q
  - Read/write (W) input signals read or write operation

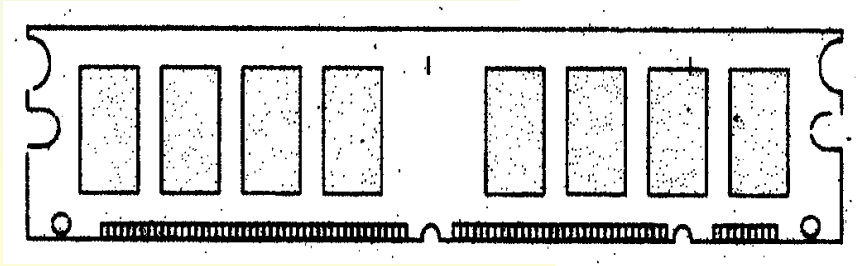
9.3 Random Access Read/Write Memories– Standard DRAM ICs

DRAM	Density (bits)	Organization
2164B	64K	64K × 1
21256	256K	256K × 1
21464	256K	64K × 4
421000	1M	1M × 1
424256	1M	256K × 4
44100	4M	4M × 1
44400	4M	1M × 4
44160	4M	256K × 16
416800	16M	8M × 2
416400	16M	4M × 4
416160	16M	1M × 16

- DRAMs are available in a variety of densities and organization
  - Typical DRAM densities
    - 64K bit
    - 256K bit
    - 1M bit, Etc.
    - Modern DRAMS as large as 1G bit
  - Typical organizations of the 4M bit DRAM
    - 4M X 1 bit
    - 1M X 4 bit
    - Modern higher density devices also available in X8, X16, and X32 organizations

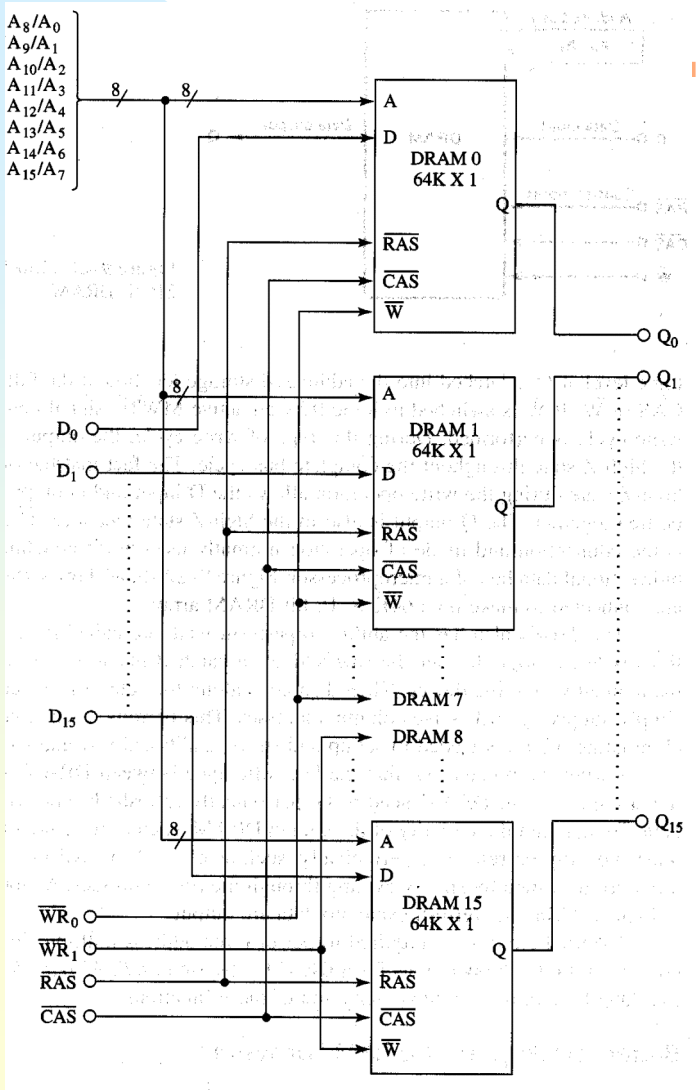
9.3 Random Access Read/Write Memories– DRAM IC Packaging





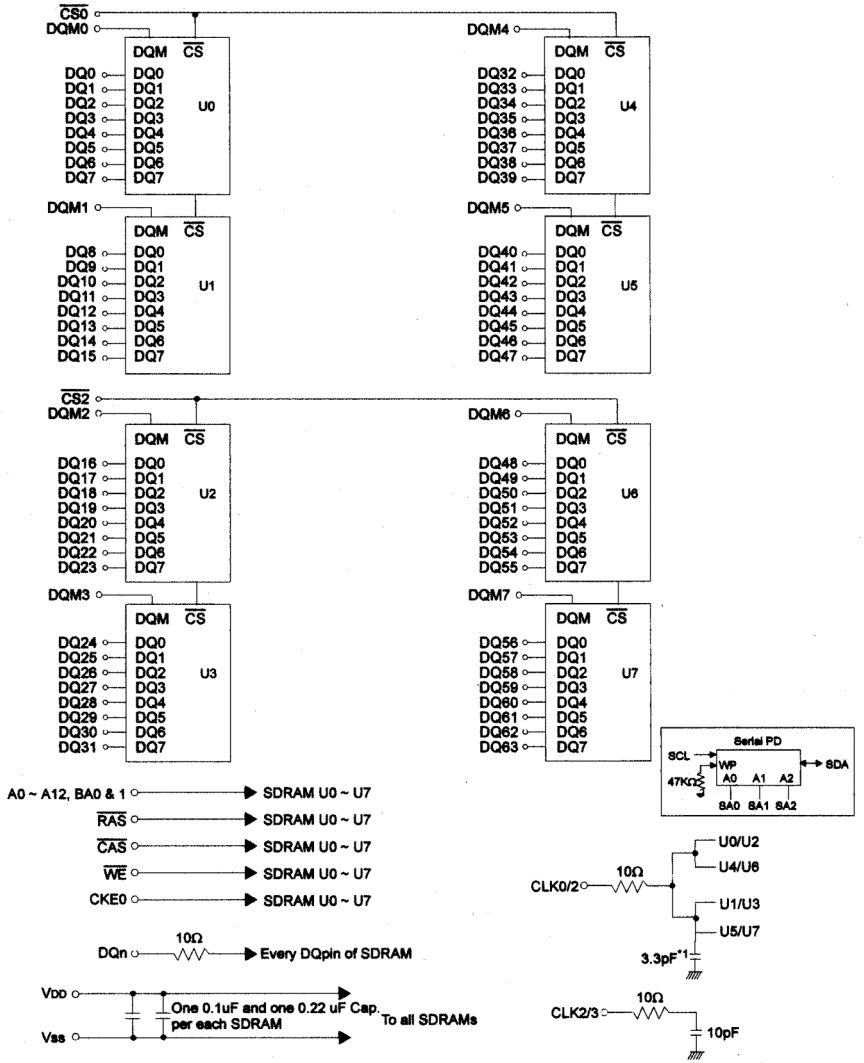
- Packaging
  - Multiplexed address permits device to be built in a package with less pins
    - Typically 16 pin DIP or 18 pin DIP
  - Modern devices available in a circuit card format—called a "module"
    - SIMM—single in-line memory module—30 pin and 72 pin versions
    - DIMM—dual in-line memory module—168pins and 184 pins
    - SIMM and DIMM differ in size, pin layout, and signal distribution
    - Permits easier upgrade of systems with more DRAM memory by simply inserting another module

9.3 Random Access Read/Write Memories– Circuit Design using DRAMS



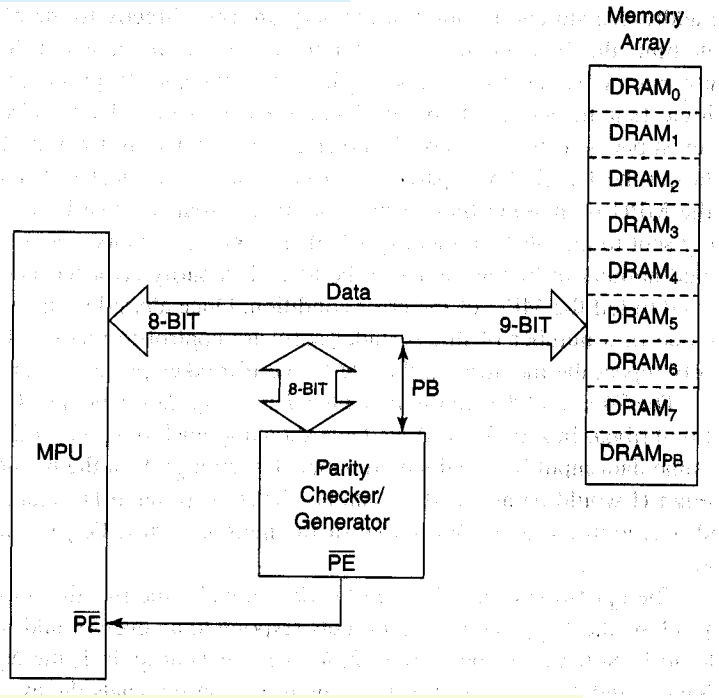
- Sixteen 64KX1-bit DRAMs interconnected to form a 64K word memory subsystem—1M-bits of memory
  - Circuit connections
    - 8 multiplexed address inputs of all devices connected in parallel
    - RAS and CAS lines of all devices connected in parallel
    - Data input and output lines
      - Independent data lines arranged to form a 16-bit wide output bus
      - Independent input lines arranged to form a 16-bit wide input bus
      - In most microprocessor applications input and output lines are connected together
    - Read/write lines
      - W inputs of upper 8 DRAMs connected together and driven by WR0*
      - W inputs of lower 8 DRAMs connected together and driven by WR1*
      - Permits byte-wide or word-wide reads and writes

9.3 Random Access Read/Write Memories– Circuitry of a DIMM Module



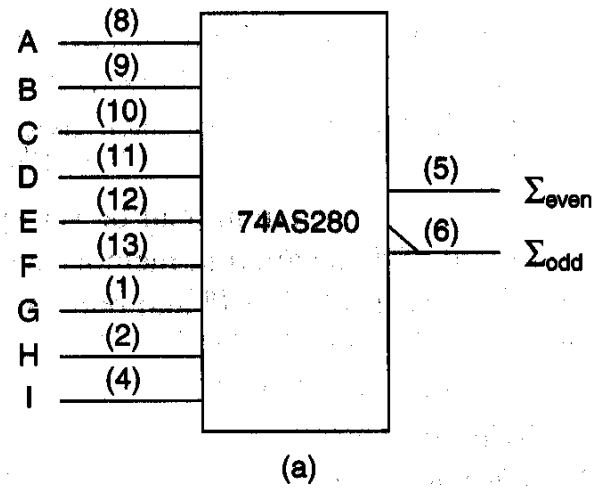
- 256M byte DIMM circuit
  - Organized 32MX64-bit or 64MX32-bit
    - Designed with 256M bit SDRAMs
      - Data transfer operations synchronized using clock (CKE) input
    - Permits connection to 32-bit or 64 bit busses
      - Connect CS_0* and CS_2* together for 64-bit-wide operation
      - Multiplexed input/outputs DQ_0-DQ_{63}
      - Input/output mask (DQM_{0-7}) inputs used to put outputs into Hi-Z state
  - Other versions available
    - With extra parity SDRMS—72 data lines

9.4 Parity, The Parity Bit, and Parity-Checker/Generator Circuit– Parity and the Parity Bit



- Data exchange between the MPU and data memory subsystem in a microcomputer must be done without error
  - Sources of errors
    - Emissions that affect data on the data bus line
    - Electrical noise signals—spikes or transients that affect data on data lines
    - Defective bit in a DRAM
    - Soft errors of DRAM
  - Solutions for improving data integrity
    - Parity
    - Error correction code (ECC)
    - Parity most frequently used
  - Parity
    - Add an additional bit of data to each byte or word of data so that all elements of data have the same parity
    - Extra bit is known as the "parity bit"
      - Even parity—element of data has an even number of bits at the 1 logic level
      - Odd parity—element of data has an odd number of bit that are logic 1
    - Circuitry added to the DRAM memory interface to generate an appropriate parity bit on writes to memory
    - Extra DRAM required to store the parity bit
    - Circuitry checks element of data from correct parity during read operations
    - Parity errors (PE) reported to MPU usually as an interrupt

9.4 Parity, The Parity Bit, and Parity-Checker/Generator Circuit– Parity Generator/Checker Circuitry



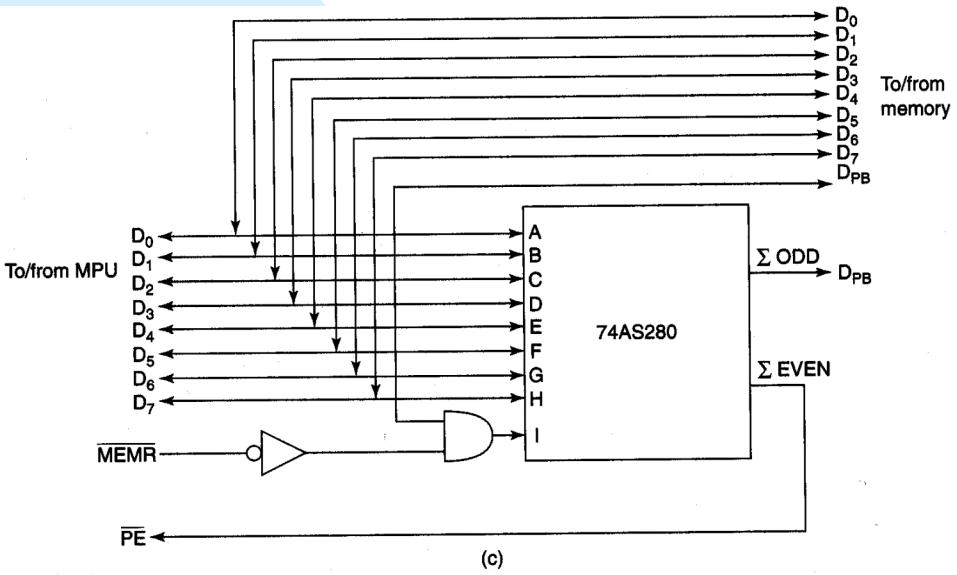
(a)

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0,2,4,6,8	H	L
1,3,5,7,9	L	H

(b)

- Parity generator/checker circuit—circuit added to the data memory interface to implement parity
  - May be implemented with a 74AS280 parity generator/checker IC
    - 9 inputs A through I
    - Two outputs Σodd and Σeven
    - Operation
      - Even number of inputs are logic 1 →
        - Σeven = 1 and Σodd = 0
        - Signals that input has even parity
      - Odd number of inputs are logic 1→
        - Σeven = 0 and Σodd = 1
        - Signals that input has odd parity

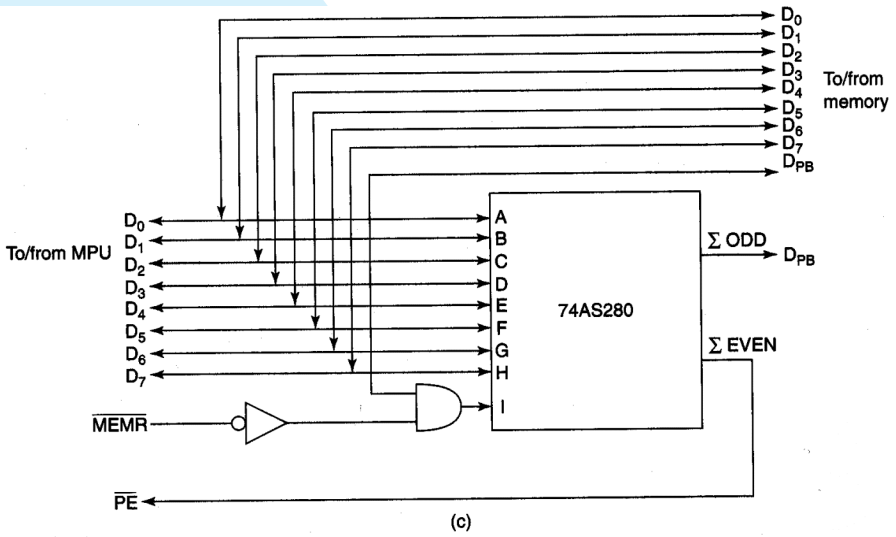
9.4 Parity, The Parity Bit, and Parity-Checker/Generator Circuit– Parity Generator/Checker Circuitry



(c)

- Even parity generator circuit
  - Circuit configuration
    - Inputs A through H attach in parallel to data bus lines D0 through D7
    - Input I is attached to the data output of the parity DRAM
      - Only activated during reads
    - Σodd output is attached to the data input of parity DRAM
  - MPU write operation
    - Accepts byte of data to be written to memory as input from the data bus
    - Data also applied in parallel to the input of the DRAMs for data lines D0 through D7
    - Circuit checks parity and generates Σodd and Σeven outputs
    - Σodd output supplied to input of parity DRAM for storage along with the byte in memory
    - If parity is even—Σodd = 0 and 9-bit value saved in memory still has even parity
    - If parity is odd—Σodd = 1 and parity of 9-bit value changed to even and saved in memory

9.4 Parity, The Parity Bit, and Parity-Checker/Generator Circuit– Parity Generator/Checker Circuitry



- Read operation:
  - Accepts 9-bit wide input from data outputs of the DRAM subsystem
  - Checks the number of bits that are at the 1 logic level
  - Produces appropriate logic level signals at odd parity and even parity outputs
    - If parity is even—Σeven = 1 and parity is correct
      - Memory operation completes normally
    - If parity is odd—Σeven = 0 and a parity error is detected
      - Error condition signaled to MPU by logic 0 at PE*
      - Usually applied as NMI input to the MPU
      - Must get serviced before executing next instruction
      - MPU may
        - Reattempt memory access
        - Initiate an orderly shut down of application

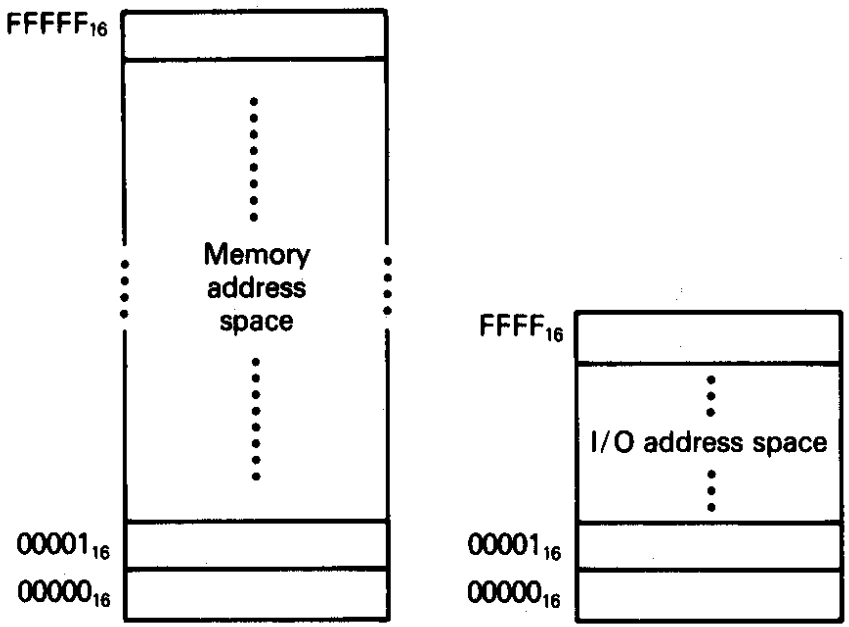
Chapter 8

The 8088 and 8086 Microprocessors—Their I/O Interface

Introduction

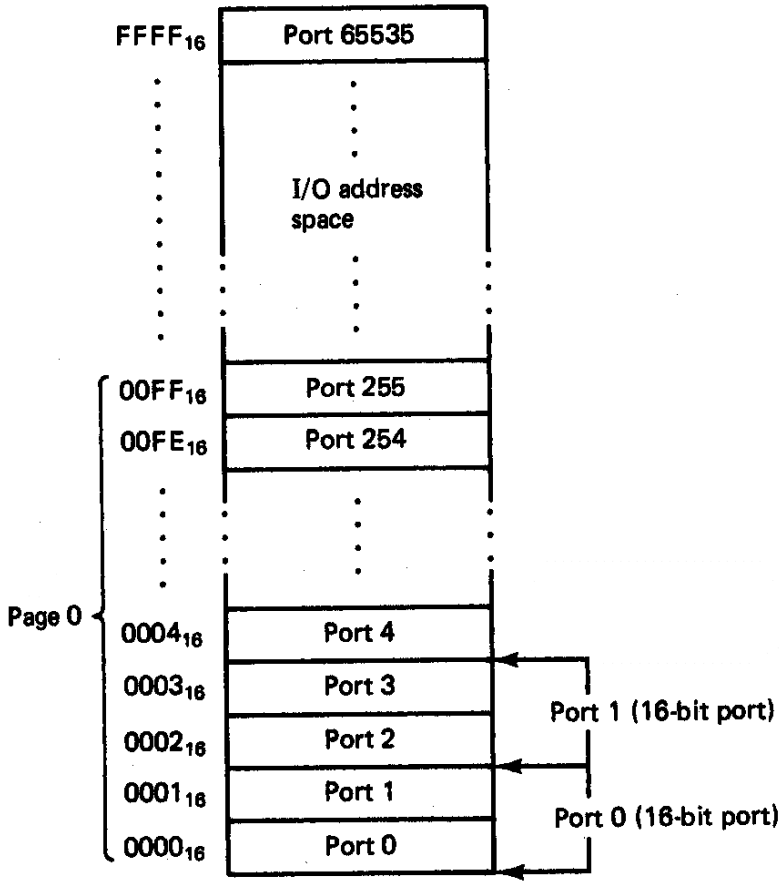
8.14 Types of Input/Output—✓
8.15 Isolated Input/Output—✓
8.16 Input/Output Data Transfers—✓
8.17 Input/Output Instructions—✓
8.18 Input/Output Bus Cycles—✓

8.14 Types of Input/Output- Role and Types of Input/Output



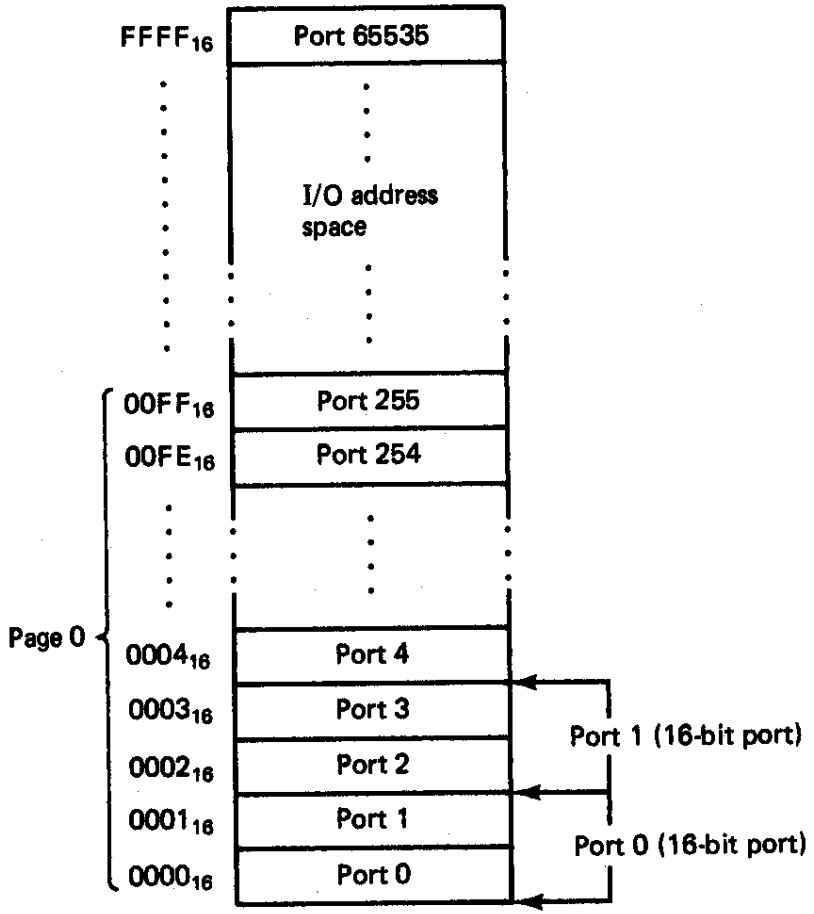
- 8088/8086 architecture implements independent memory and input/output address spaces
  - Memory address space- 1,048,576 bytes long (1M-byte)—00000H-FFFFFH
  - Input/output address space- 65,536 bytes long (64K-bytes)—0000H-FFFFH
  - Input/output can be implemented in either the memory or I/O address space
- Role of I/O
  - Allows I/O devices such as peripheral ICs to input data or receive results
  - Each input/output address is called a port
  - An I/O device may be assigned a range of I/O ports
- Types of Input/Output
  - Isolated I/O– ports implemented in the I/O address space
  - Memory mapped I/O—ports implemented in the memory address space
  - Microcomputer systems can employ both types

8.14 Real-Mode Input-Output Address Space- Isolated I/O



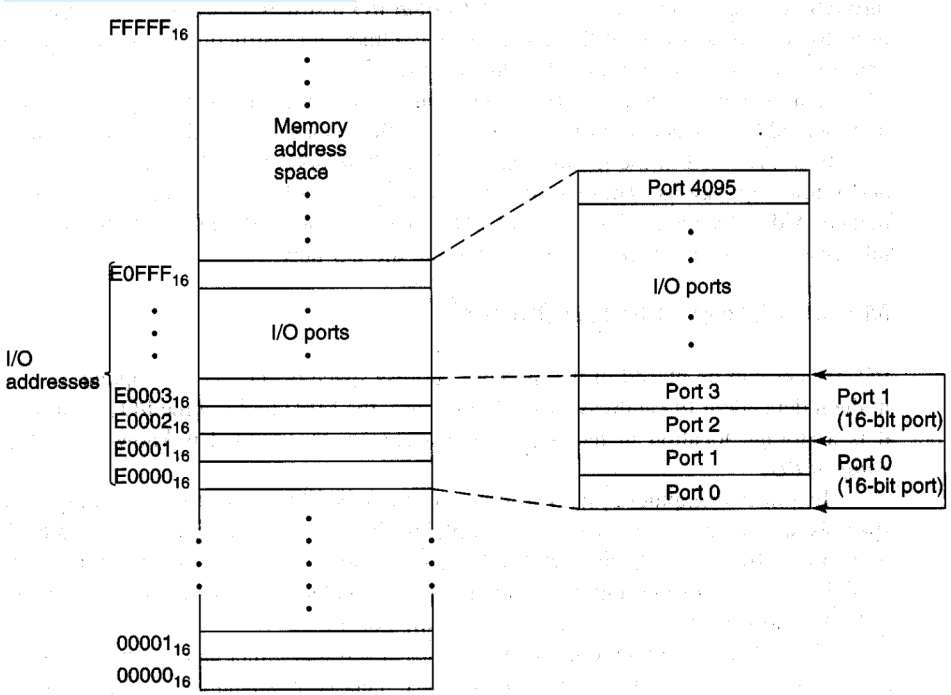
- Input/output data organization
  - Supports byte and word I/O ports
    - 64K independent byte-wide I/O ports
    - 32K independent aligned word-wide I/O ports
    - Word ports may also be misaligned
  - Examples:
    Byte ports 0,1,2 → addresses 0000H, 0001H, and 0002H
    Word ports 0,1,2 → addresses 0000H, 0002H, 0004H
- Advantages of isolated I/O
  - Complete memory address space available for use by memory
  - I/O instructions tailored to maximize performance
- Disadvantage of Isolated I/O
  - All inputs/outputs must take place between an I/O port and accumulator register

8.14 Real-Mode Input-Output Address Space- Isolated I/O (Continued)



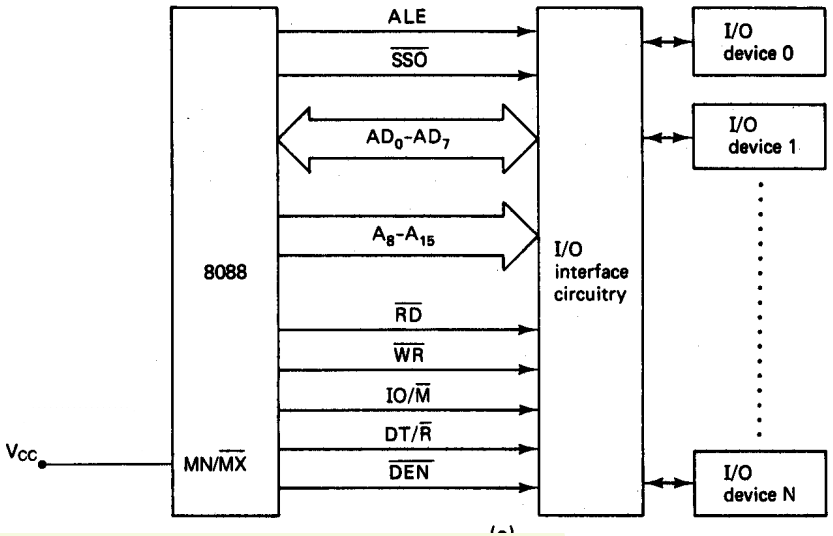
- All I/O accesses take either one or two bus cycles
  - Byte input/output= 1 bus cycle
  - Aligned word input/output= 1 bus cycle—on 8086
  - Misaligned word input/output = 2 bus cycles
- Page 0
  - First 256 byte addresses→ 0000H - 00FFH
  - Can be accessed with direct or variable I/O instructions
  - Ports F8H through FFH reserved

8.14 Input-Output Address Space- Memory Mapped I/O



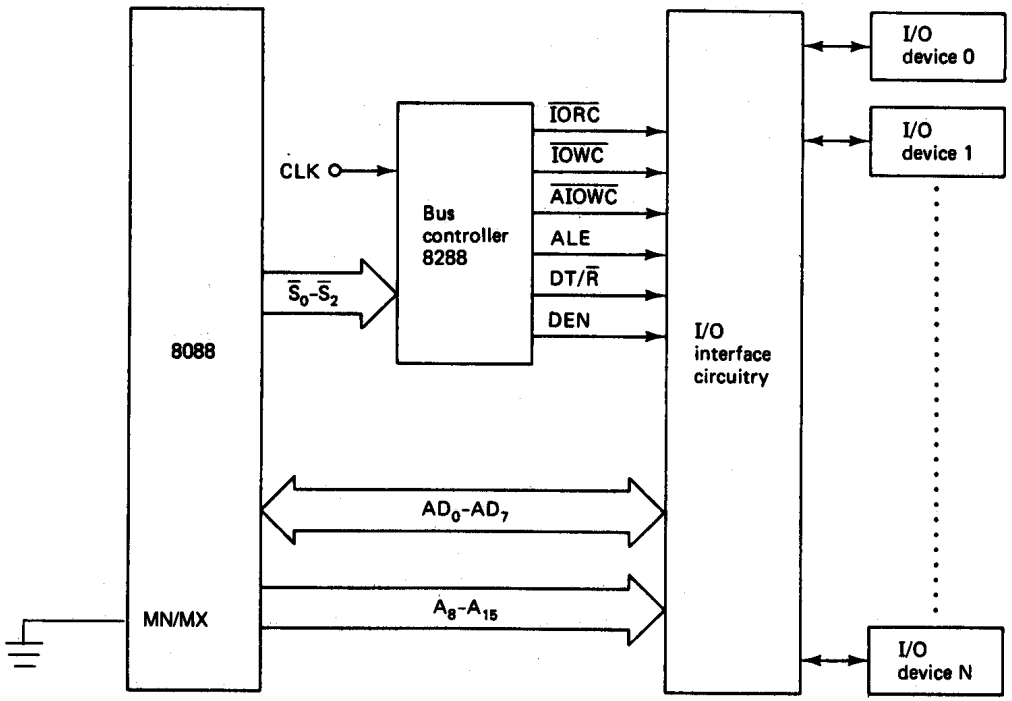
- Memory mapped I/O—a part of the memory address space is dedicated to I/O devices
  - Example:
    - E0000H-E0FFFH → 4096 memory addresses assigned to I/O ports
      - E0000H, E0001H, and E0002H correspond to byte-wide ports 0,1, and 2
      - E0000H and E0001H correspond to word-wide port 0 at address E0000H
- Advantages of memory mapped I/O
  - Instructions that affect data in memory (MOV, ADD, AND, etc.) can be used to perform I/O operations
  - I/O transfers can take place between and I/O port and any of the registers
- Disadvantage of memory mapped I/O
  - Memory instructions perform slower
  - Part of the memory address space cannot be used to implement memory

8.15 Isolated Input/Output Interface– 8088 Minimum-Mode Interface



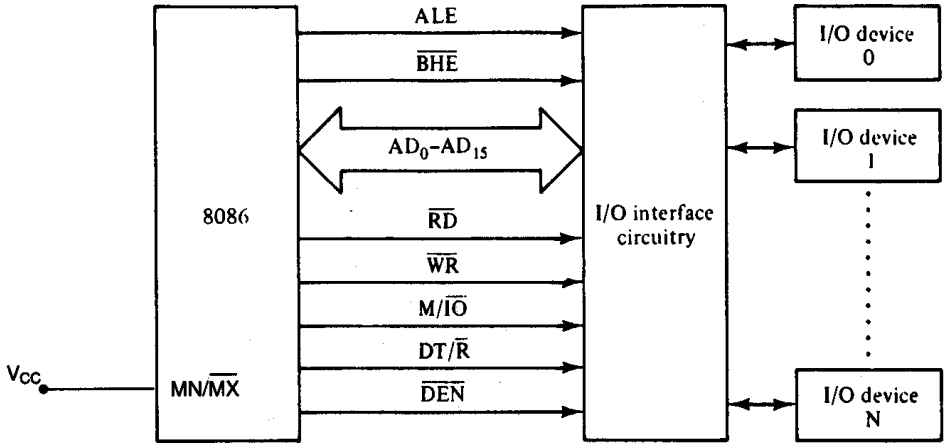
- Similar in structure and operation to memory interface
- I/O devices—can represent LEDs, switches, keyboard, serial communication port, printer port, etc.
- I/O data transfers take place between I/O devices and MPU over the multiplexed-address data bus
  - AD0-AD7
  - A8-A15
- Control signal review
  - ALE = pulse to logic 1 tells bus interface circuitry to latch I/O address
  - RD* = logic 0 tells the I/O interface circuitry that an input (read) is in progress
  - WR*= logic 0 tells the I/O interface circuitry that an output (write) is in progress
  - IO/M*= logic 1 tells I/O interface circuits that the data transfer operation is for the IO subsystem
  - DT/R* = sets the direction of the data bus for input (read) or output (write) operation
  - DEN*= enables the interface between the I/O subsystem and MPU data bus

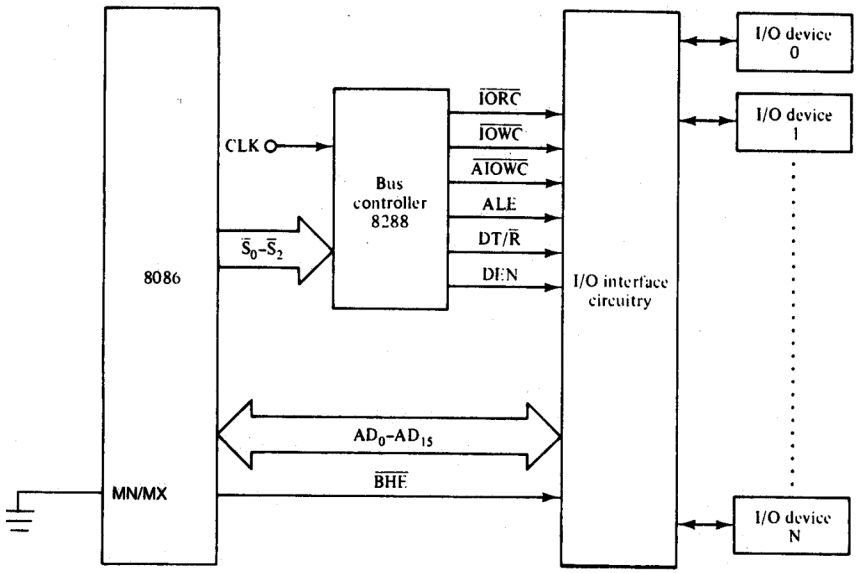
8.15 Isolated Input/Output Interface– 8088 Maximum-Mode Interface



- Maximum-mode interface differences review
  - 8288 bus controller produces the control signals
  - Signal changes
    - IORC* replaces RD*
    - IOWC* and AIOWC* replace WR*
    - DEN is complement of DEN*
    - IO/M* no longer needed (bus controller creates separate IO read/write controls)
    - SSO* no longer part of interface

8.15 Isolated Input/Output Interface– 8086 Minimum and Maximum-Mode Interfaces





8.15 I/O Control Signals– 8088/8086 Maximum-Mode Bus Status Codes

Status inputs			CPU cycle	8288 command
$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$		
0	0	0	Interrupt acknowledge	$\overline{INTA}$
0	0	1	Read I/O port	$\overline{IORC}$
0	1	0	Write I/O port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction fetch	$\overline{MRDC}$
1	0	1	Read memory	$\overline{MRDC}$
1	1	0	Write memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

- Bus status code review
  - During all I/O accesses one of two bus cycle status code are output by the MPU
    - Read I/O port
    - Write I/O port
  - 8288 decodes to produce appropriate control command signals
    - IORC* → input (read I/O)
    - IOWC* → output (write I/O)
    - AIOWC* → output (write I/O)

8.17 Input/Output Instructions– Direct I/O Instructions

Mnemonic	Meaning	Format	Operation
IN	Input direct	IN Acc,Port	(Acc) ← (Port) Acc = AL or AX
	Input indirect (variable)	IN Acc,DX	(Acc) ← ((DX))
OUT	Output direct	OUT Port,Acc	(Port) ← (Acc)
	Output indirect (variable)	OUT DX,Acc	((DX)) ← (Acc)

- Types of instructions
  - Direct I/O instructions—only allow access to ports at page 0 addresses
  - Variable I/O instructions—allows access of ports anywhere in the I/O address space
- Direct I/O instructions

  IN Acc,Port

  OUT Port,Acc
  - Port = 8-bit direct address—limited to 0H through FFH (page 0)
  - Acc = accumulator register AX (word transfer); AH or AL (byte transfer)
  - Example:

    IN AL, 0FEH

    (FE) → AL (byte input operation)
- Also known as accumulator I/O—because source or destination must always be in accumulator (A) register

8.17 Input/Output Instructions– Variable I/O Instructions

Mnemonic	Meaning	Format	Operation
IN	Input direct	IN Acc,Port	(Acc) ← (Port) Acc = AL or AX
	Input indirect (variable)	IN Acc,DX	(Acc) ← ((DX))
OUT	Output direct	OUT Port,Acc	(Port) ← (Acc)
	Output indirect (variable)	OUT DX,Acc	((DX)) ← (Acc)

- Variable I/O instructions

  IN Acc,DX

  OUT DX,Acc

  - DX = 16-bit indirect address—allows access to full I/O address space
  - Acc = accumulator register AX (word transfer); AH or AL (byte transfer)
  - Example:

    MOV DX,0A000H ;load I/O address

    IN AL,DX ;input value to AL

    MOV BL,AL ;copy value to BL

(A000H) → BL (byte input operation)

8.17 Input/Output Instructions– Examples

- Write instructions to output the value FFH to the byte wide port at I/O address ABH

- Solution:

```
MOV AL, 0FFH ;load data into AL
OUT  0ABH,AL  ;output to port ABH
```

- Write instructions to output the value FFH to the byte wide port at I/O address B000H

- Solution:

```
MOV DX,0B000H ; load address into DX
MOV AL, 0FFH    ; load data into AL
OUT  DX,AL        ; output to port B000H
```

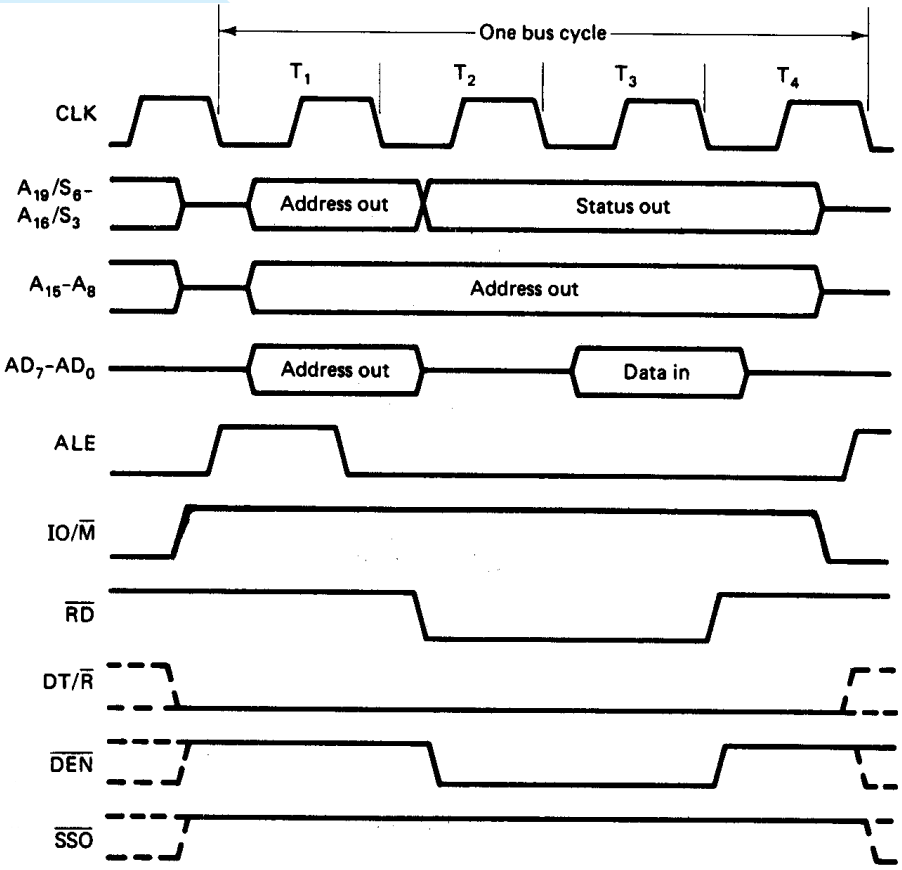
8.17 Input/Output Instructions– Examples (Continued)

- Read data from byte-wide ports at addresses AAH and A9H. Output as a word to the word-wide port at address B000H.

- Solution:

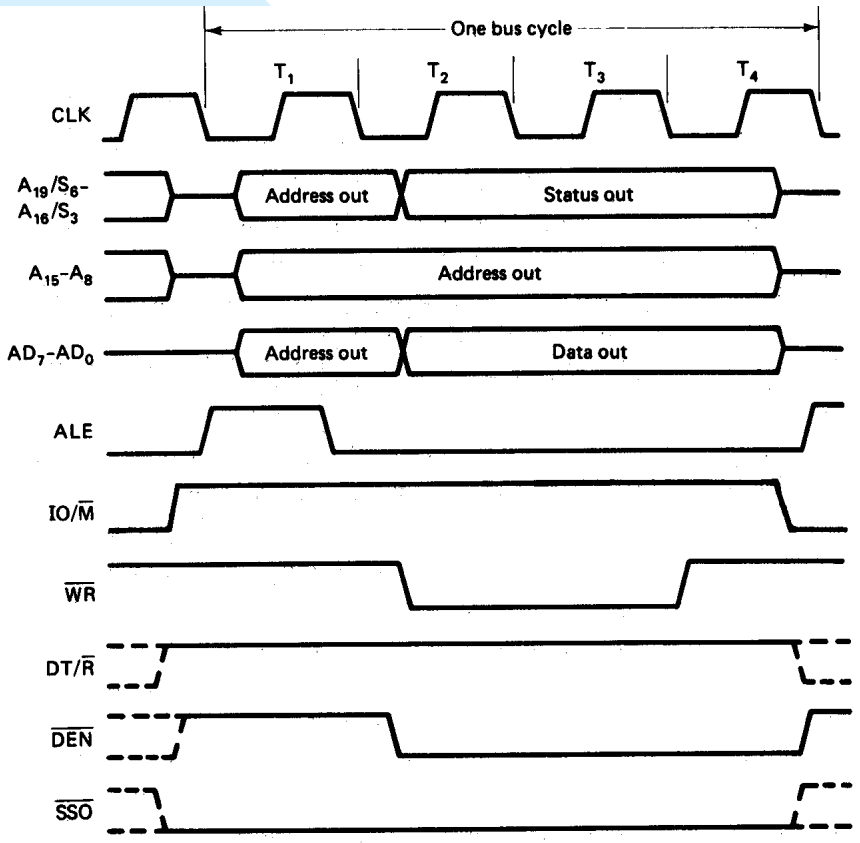
```
IN  AL,0AAH        ; input first byte
MOV AH, AL         ; load data into AL
IN  AL,0A9H        ; input 2nd byte
MOV DX,0B000H ; load address into DX
OUT  DX,AX         ; output word to port B000H
```

8.18 Input and Output Bus Cycles– 8088
Minimum Mode Input Bus Cycle



- Input (I/O read) bus cycle timing diagram—shows relationship between signals relative to time states
  - T1 state—input cycle begins
    - Address output on A0-A15
    - Pulse produced at ALE--address should be latched in external circuitry on trailing edge of ALE
    - IO/M* set to 1→ I/O bus cycle
    - DT/R* set to 0→ set external data bus control circuitry for receive mode (input)
  - T2 state
    - Status code output on S3-S6
    - AD0 through AD7 tri-stated in preparation for data bus operation
    - RD* set to 0→ input cycle
    - DEN* set to 0 → enable external data bus control circuitry
  - T3 state
    - Data on D0-D7 input (read) by the MPU
  - T4 state—input cycle finishes
    - RD* returns to 1→ inactive level
    - Complete address/data bus tri-stated
    - IO/M* returned to 0 → memory bus cycle
    - DEN* returned to 1→ inactive level
    - DT/R* returns to 1→ transmit level

8.18 Input and Output Bus Cycles– 8088
Minimum Mode Output Bus Cycle



- Output (I/O write) bus cycle timing diagram
  - T1 state—output cycle begins
    - Address output on A0-A15
    - Pulse produced at ALE and address latched in external circuitry on trailing edge of ALE
    - IO/M* set to 1→ I/O bus cycle
    - DT/R* set to 1→ external data bus control circuitry for transmit mode (output)
  - T2 state
    - Status code output on S3-S6
    - AD0 through AD7 transitioned to data bus and output data placed on bus
    - DEN* set to 0 → enable external data bus control circuitry
    - WR* set to 0→ output cycle
  - T3 or T4 state
    - Data on D0-D7 output (write) into I/O port (I/O device decides when!)
  - T4 state—output cycle finishes
    - WR* returns to 1→ inactive level
    - Complete address/data bus tri-stated
    - IO/M* returned to 0 → memory bus cycle
    - DEN* returned to 1→ inactive level

8.18 Input and Output Bus Cycles– 8086 Minimum Mode Read and Write Bus Cycles