Chapter 8
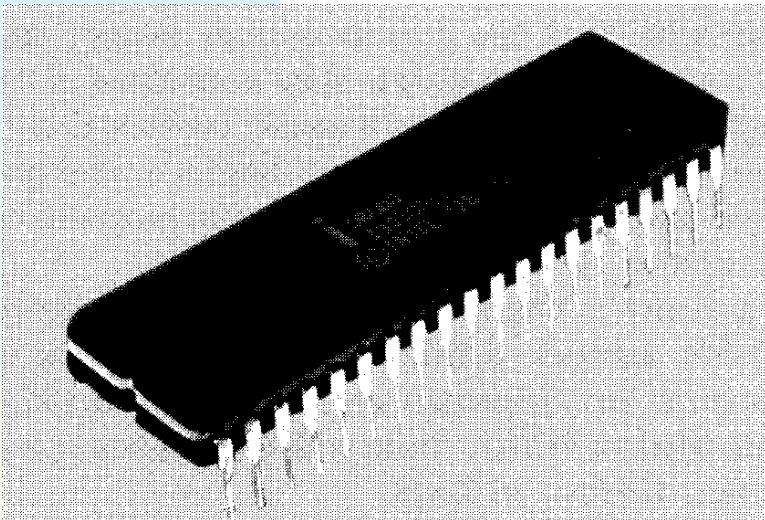
The 8088 and 8086 Microprocessors—Their Memory Interface

Introduction

# 8.1   8088 and 8086 Microprocessors– Introduction

- First generation 16-bit microprocessor from Intel Corporation
  - 8086 Microprocessor—1979
    - Full 16-bit architecture
    - Internally processed 16-bit data
    - Externally accessed 16-bit wide data memory
  - 8088 Microprocessor—1980
    - Processed 16-bit data internally/accessed 8-bit wide data memory externally
    - Permitted lower cost system solution
    - Resulted in lower performance
  - Common characteristics
    - Manufactured on high-performance metal-oxide process (HMOS)
    - Circuitry equivalent to 29000 transistors
    - 40 pin dual-in-line (DIP) package

8.1 8088 and 8086 Microprocessors– Pin Functions
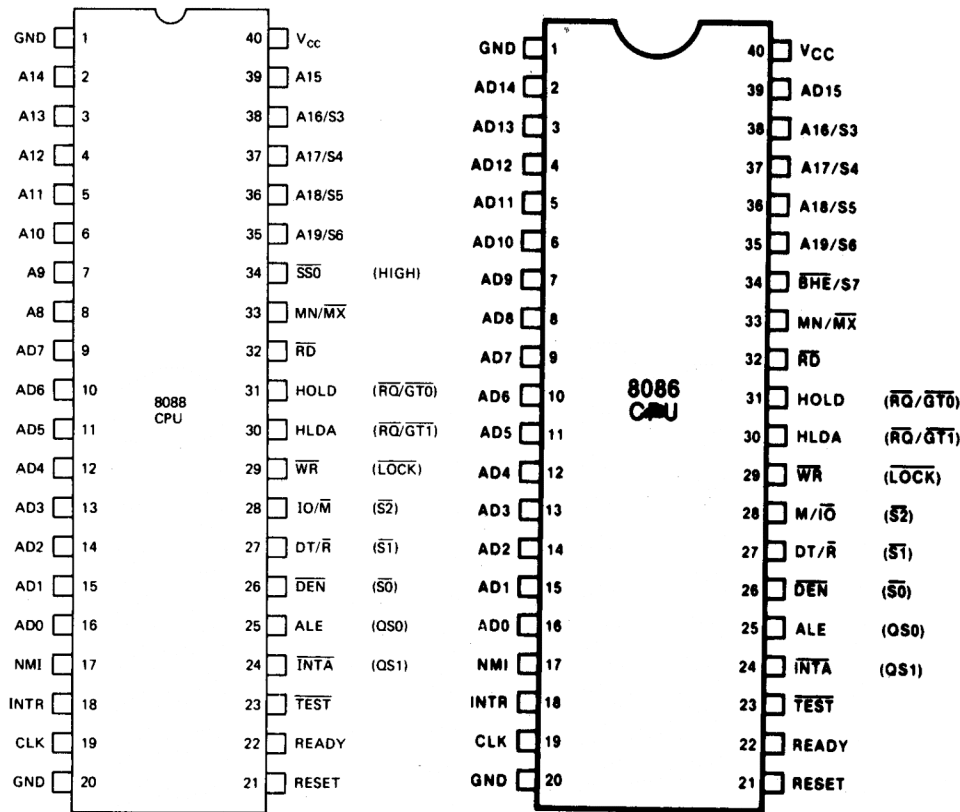
■ **Pin functions**

- **Most pins are independent and serve a single function**
  - **Examples:**
    CLK—clock
    INTR—interrupt request
    READY—bus ready
- **Some multi-functions pins– different times/different mode**
  - **Examples:**
    AD0-AD15– multiplexed address/data lines at different times
    A16/S3—multiplexed address and status line at different times
    IO/M* or S2* Control line in one mode or bus status line in other mode

8.2 Minimum-Mode and Maximum-Mode Systems– Selecting the Mode and Types of Signals

Common signals		
Name	Function	Type
AD7–AD0	Address/data bus	Bidirectional, 3-state
A15–A8	Address bus	Output, 3-state
A19/S6–A16/S3	Address/status	Output, 3-state
MN/MX̄	Minimum/maximum Mode control	Input
R̄D̄	Read control	Output, 3-state
T̄ĒST̄	Wait on test control	Input
READY	Wait state control	Input
RESET	System reset	Input
NMI	Nonmaskable Interrupt request	Input
INTR	Interrupt request	Input
CLK	System clock	Input
Vcc	+5 V	Input
GND	Ground	

(a)

Minimum mode signals (MN/MX̄ = Vcc)		
Name	Function	Type
HOLD	Hold request	Input
HLDA	Hold acknowledge	Output
W̄R̄	Write control	Output, 3-state
IO/M̄	IO/memory control	Output, 3-state
DT/R̄	Data transmit/receive	Output, 3-state
D̄ĒN̄	Data enable	Output, 3-state
S̄S̄Ō	Status line	Output, 3-state
ALE	Address latch enable	Output
ĪN̄T̄Ā	Interrupt acknowledge	Output

(b)

Maximum mode signals (MN/MX̄ = GND)		
Name	Function	Type
R̄Q̄/ḠT̄1, 0	Request/grant bus access control	Bidirectional
L̄Ō̄C̄K̄	Bus priority lock control	Output, 3-state
S̄2̄-S̄0̄	Bus cycle status	Output, 3-state
QS1, QS0	Instruction queue status	Output

(c)

- Two operating modes of 8088/8086
  - Minimum mode—small system/single processor configuration
  - Maximum mode—large system/single-multi-processor configuration
  - Hardware connection at MN/MX* pin 33 selects mode
    - 1 = +Vcc = Minimum mode
    - 0 = GND = Maximum mode
  - 8088 signals/pins categorized as
    - Common—same function both modes
      Examples: Pin 9 (AD7)- pin 16 (AD0)
    - Minimum Mode—special minimum mode operations
      Examples: pins 26-28 are DEN*, DT/R*, and IO/M*
    - Maximum Mode—special maximum mode operations
      Example: pins 26-28 are S0*, S1*, and S2*

8.3 Minimum-Mode Interfaces– 8088 Interface

Power supply

V$_{CC}$ GND

Address/data bus

INTR

$\overline{INTA}$

Interrupt interface

$\overline{TEST}$

NMI

RESET

8088 MPU

DMA interface

HOLD

HLDA

V$_{CC}$

Mode select

MN/$\overline{MX}$

CLK

Clock

AD$_0$-AD$_7$, A$_{16}$/S$_3$-A$_{19}$/S$_6$

A$_8$-A$_{15}$

ALE

$\overline{SSO}$

IO/$\overline{M}$

DT/$\overline{R}$

$\overline{RD}$

$\overline{WR}$

$\overline{DEN}$

READY

Memory/IO controls

- ■ Minimum Mode Interface
  - MPU provides all of the interface signals
    - Address/data bus
    - Status
    - Control
    - Interrupt
    - DMA
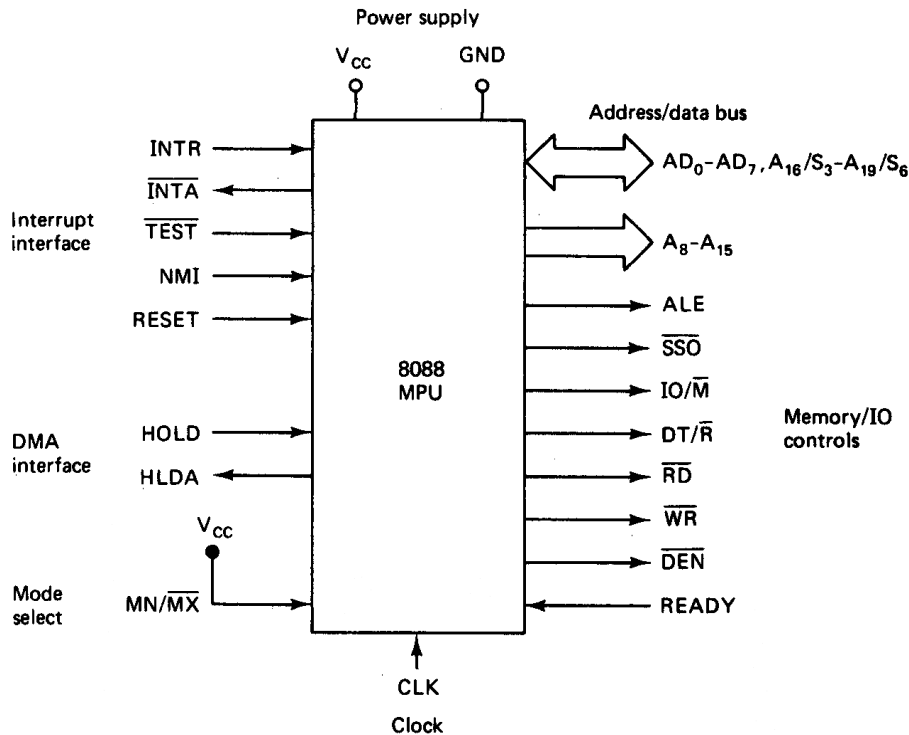- Multiplexed address/data bus
  - 20-bit address (A19-A0) → 1MByte address space
  - 8-bit data bus (D7-D0)
  - Signals of the address/data bus
    - AD0-AD7—bi-directional, tri-state
      - Lower 8 address output lines
      - 8 bi-directional data bus lines
    - A8-A15—output, tri-state
      - Next 8 address lines
    - A16/S3-A19/S6—output, tri-state
      - Four most significant address lines
      - S3–S6 status outputs
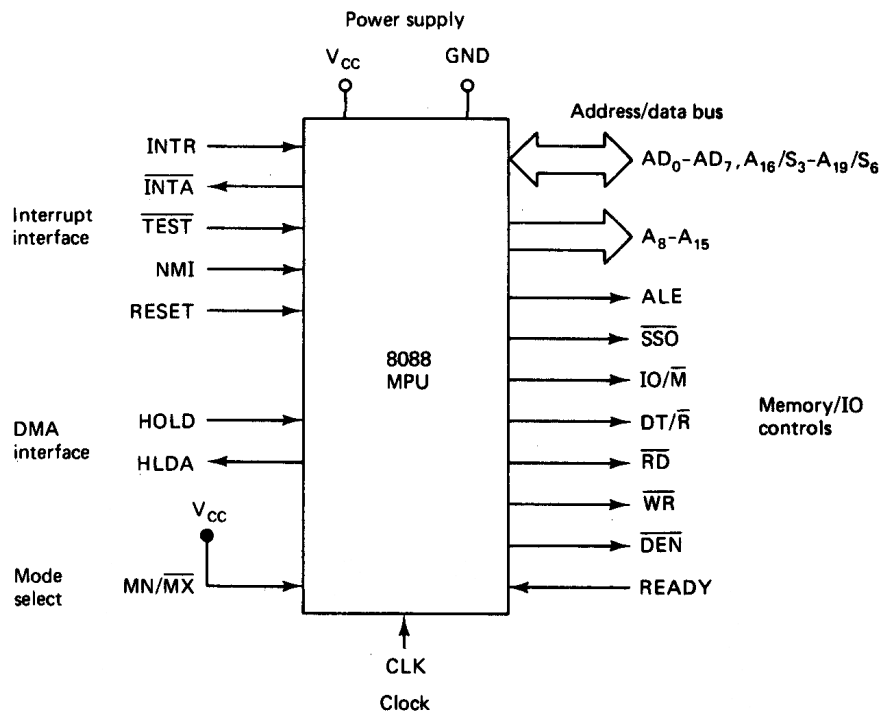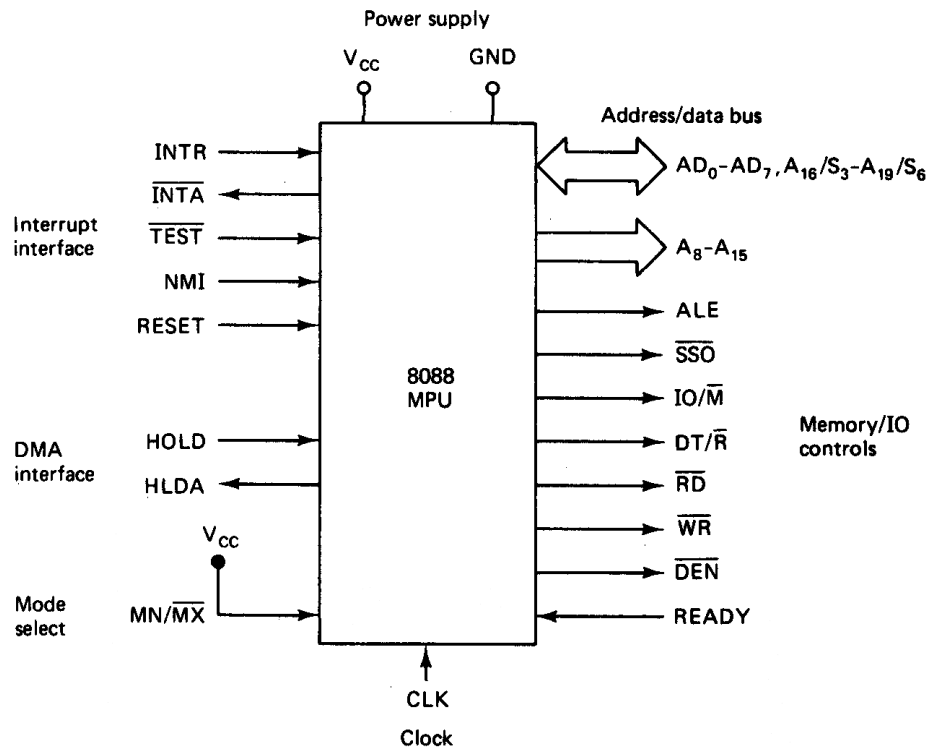
8.3 Minimum-Mode Interfaces– 8088 Interface

- **Memory/IO Control Signals**
  - **Support signals for controlling the memory and I/O interface circuitry**
    - **All but READY are outputs**
  - **ALE= address latch enable**
    - **Signals external circuitry that a valid address in on the address bus and it should be latched**
  - **IO/M* = IO/memory**
    - **Identifies type of data transfer taking place over the data bus; used to enable/disable memory and/or IO interface**
      - **IO/M* = 1 = input/output data**
      - **IO/M* = 0 = memory data**
  - **DT/R* = data transmit/receive**
    - **Tells external circuitry which way data is to be transferred over the bus; used to set direction of data bus interface circuits**
      - **DT/R* = 1 = transmit mode (write/output)**
      - **DT/R* = 0 = read mode (read/input)**

Power supply

V_{CC} GND

Address/data bus

INTR

$\overline{INTA}$

$\overline{TEST}$

NMI

RESET

Interrupt interface

AD_0–AD_7, A_{16}/S_3–A_{19}/S_6

A_8–A_{15}

ALE

$\overline{SSO}$

IO/$\overline{M}$

8088 MPU

HOLD

HLDA

DMA interface

V_{CC}

MN/$\overline{MX}$

Mode select

DT/$\overline{R}$

$\overline{RD}$

$\overline{WR}$

$\overline{DEN}$

READY

Memory/IO controls

CLK

Clock

Power supply

V_CC   GND

INTR

$\overline{\text{INTA}}$

$\overline{\text{TEST}}$ Interrupt interface

NMI

RESET

8088 MPU

HOLD   DMA interface

HLDA

V_CC

MN/$\overline{\text{MX}}$ Mode select

CLK

Clock

Address/data bus

AD_0-AD_7, A_{16}/S_3-A_{19}/S_6

A_8-A_{15}

ALE

$\overline{\text{SSO}}$

IO/$\overline{\text{M}}$

DT/$\overline{\text{R}}$ Memory/IO controls

$\overline{\text{RD}}$

$\overline{\text{WR}}$

$\overline{\text{DEN}}$

READY

- Memory/IO Control Signals (continued)
  - RD* = read → active 0
    - Signals that a read/input bus cycle is in progress
  - WR* = write → active 0
    - Signals that a write/output bus cycle is in progress
  - DEN* = data enable → active 0
    - Signal when the data bus should be enabled
  - READY = ready
    - 1= Acknowledges that the memory subsystem is ready to complete the bus cycle
    - 0= Memory subsystem is not ready; insert wait sates to extend the bus cycle
  - SSO* = status
    - 0= instruction code read
    - 1= data access

8.3 Minimum-Mode Interfaces– 8088 Interface

Power supply

V_CC GND

Address/data bus

INTR

$\overline{INTA}$

Interrupt interface

$\overline{TEST}$

NMI

RESET

8088 MPU

$AD_0-AD_7, A_{16}/S_3-A_{19}/S_6$

A_8-A_{15}

ALE

$\overline{SSO}$

$IO/\overline{M}$

$DT/\overline{R}$

$\overline{RD}$

$\overline{WR}$

$\overline{DEN}$

READY

Memory/IO controls

DMA interface

HOLD

HLDA

V_CC

Mode select

MN/$\overline{MX}$

CLK

Clock

- **Interrupt Interface**
  - **Support signals for implementing an interrupt driven I/O interface**
    - **Maskable interrupt interface—INTR and INTA***
    - **Nonmaskable interrupt interface—NMI**
    - **Reset interface—RESET**
  - **INTR = interrupt request input → active 1 (level triggered)**
    - **External device signals the MPU that it needs maskable interrupt service**
  - **INTA* = interrupt acknowledge output→ active 0**
    - **MPU acknowledges to an external devices that its maskable interrupt request is being serviced**
  - **NMI = nonmaskable interrupt input**
    - **External device initiates NMI request with 0 to 1 transition (edge triggered)**
  - **RESET = reset input → active 1**
    - **Logic 1 initiates hardware reset of MPU**
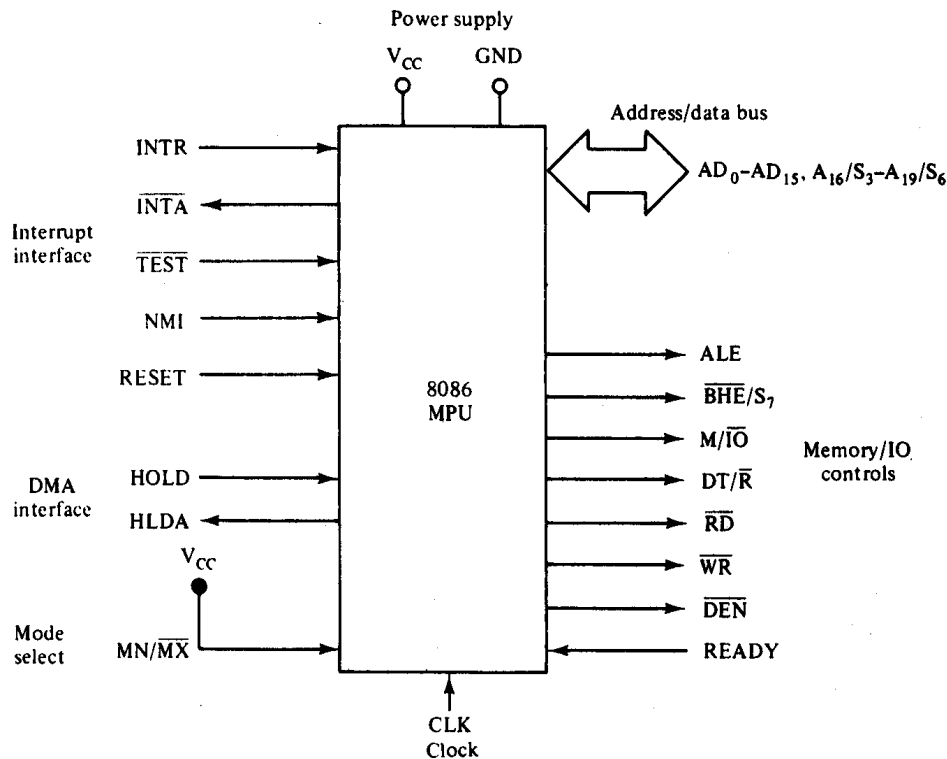   - **Initializes internal registers and reset service routine**

The 8088 and 8086 Microprocessors, Triebel and Singh   9

8.3 Minimum-Mode Interfaces– 8088 Interface

Power supply

V_{CC} GND

Address/data bus

INTR

$\overline{INTA}$

Interrupt interface

$\overline{TEST}$

NMI

RESET

8088 MPU

AD_0-AD_7,A_{16}/S_3-A_{19}/S_6

A_8-A_{15}

ALE

$\overline{SSO}$

IO/$\overline{M}$

DT/$\overline{R}$

$\overline{RD}$

$\overline{WR}$

$\overline{DEN}$

READY

Memory/IO controls

DMA interface

HOLD

HLDA

V_{CC}

Mode select

MN/$\overline{MX}$

CLK

Clock
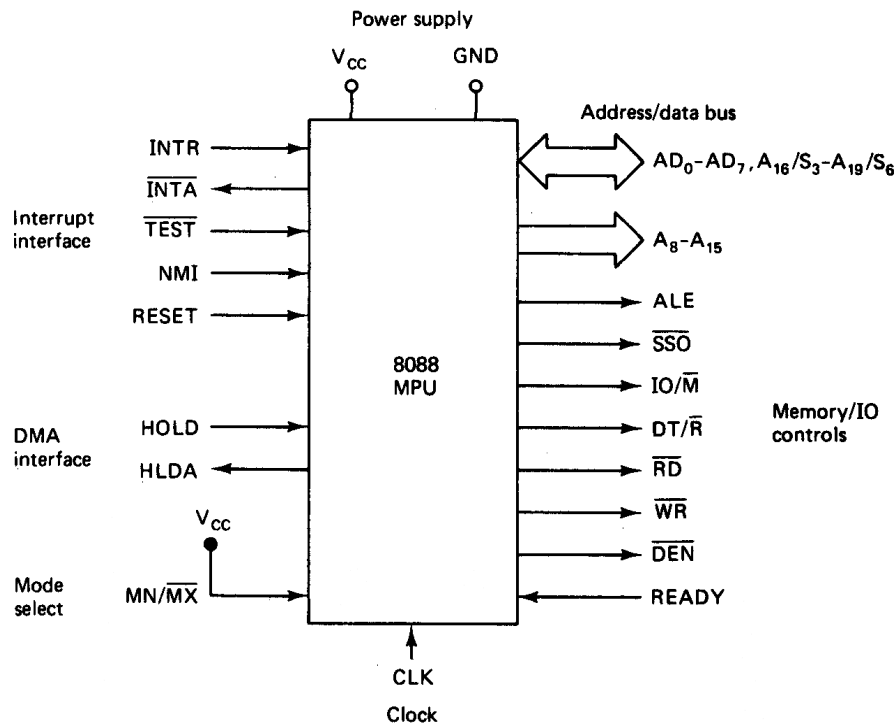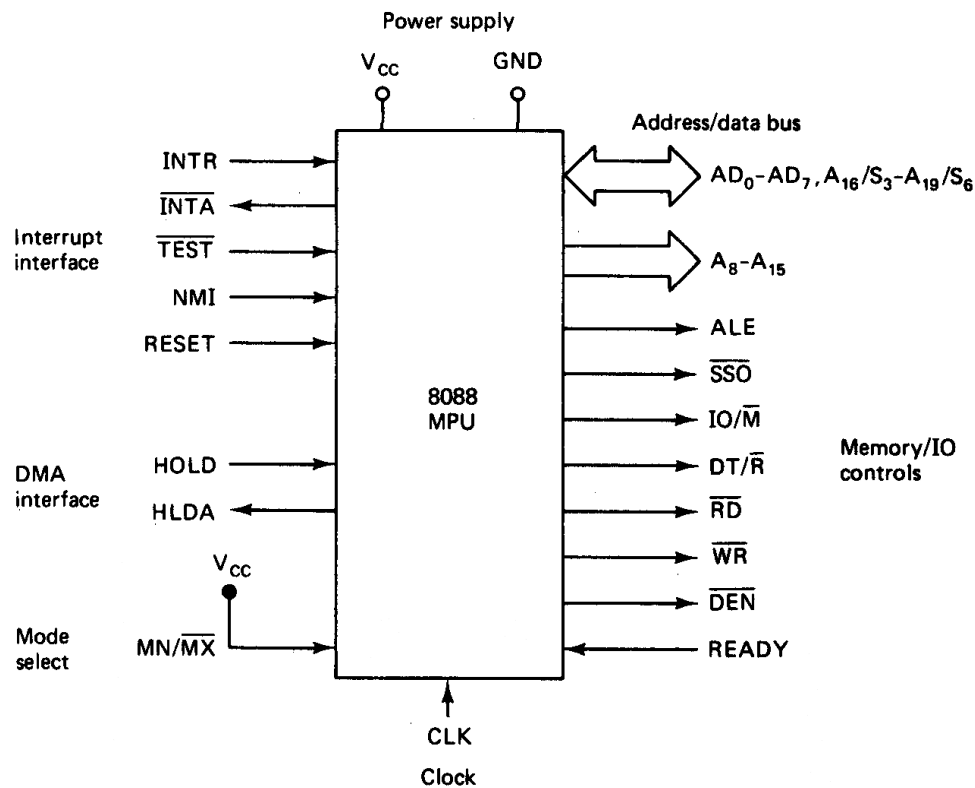
- Direct Memory Access Interface
  - Support signals for implemented a direct memory access interface
    - Permits direct transfer of information between parts of memory or between memory and I/O devices
    - External devices, such as a DMA controller, perform these operations independent of MPU
  - HOLD= Hold request input → active 1 (level triggered)
    - External device request the MPU give it control of the system bus
  - HOLDA* = Hold acknowledge output→ active 1
    - MPU tri-states its bus lines
    - Acknowledges to an external devices that the MPU bus is in the hold state

8.3 Minimum-Mode Interfaces– 8086 Interface Differences

Power supply

V_CC   GND

Address/data bus

AD_0-AD_{15}, $A_{16}/S_3-A_{19}/S_6$

INTR

$\overline{INTA}$

Interrupt interface

$\overline{TEST}$

NMI

RESET

8086 MPU

ALE

$\overline{BHE}/S_7$

$M/\overline{IO}$

Memory/IO controls

DT/$\overline{R}$

$\overline{RD}$

$\overline{WR}$

$\overline{DEN}$

READY

DMA interface

HOLD

HLDA

V_CC

Mode select

MN/$\overline{MX}$

CLK Clock

- **Data bus**
  - **16-bit wide**
    - **D15-D0**
    - **Multiplexed with A15 through A0**
    - **Allows 3 types of data transfers**
      - **Word—over D15-D0**
      - **Low byte—over D7-D0**
      - **High byte—over D15-D8**
  - **Memory/IO Controls**
    - **SSO* → BHE* (bank high enable)**
      - **Used to signal external circuitry whether or not a byte transfer is taking place over the upper 8 data bus lines**
    - **A0 now does the same for a byte transfer over the lower 8 data bus line**

8.4 Maximum-Mode Interfaces– 8088 Interface

- **Intended for use in multi-processor applications**
  - **Multiple 8088/8086 MPU**
  - **Floating point coprocessor**
  - **Global versus local resources**
    - **Local resource (memory, IO, etc.) only accessible by a specific processor**
    - **Global resources are shared by all processors**
    - **Global resources can only be access by one MPU at a time; access requires bus locking**
    - **New signal LOCK* is used by MPU to lock other processors off the bus during an access of a global resource**
  - **Maximum-mode configuration**
    - **MN/MX* pin = 0 → GND**
    - **Most memory, IO, and interrupt interface outputs produced by an external 8288 bus controller**
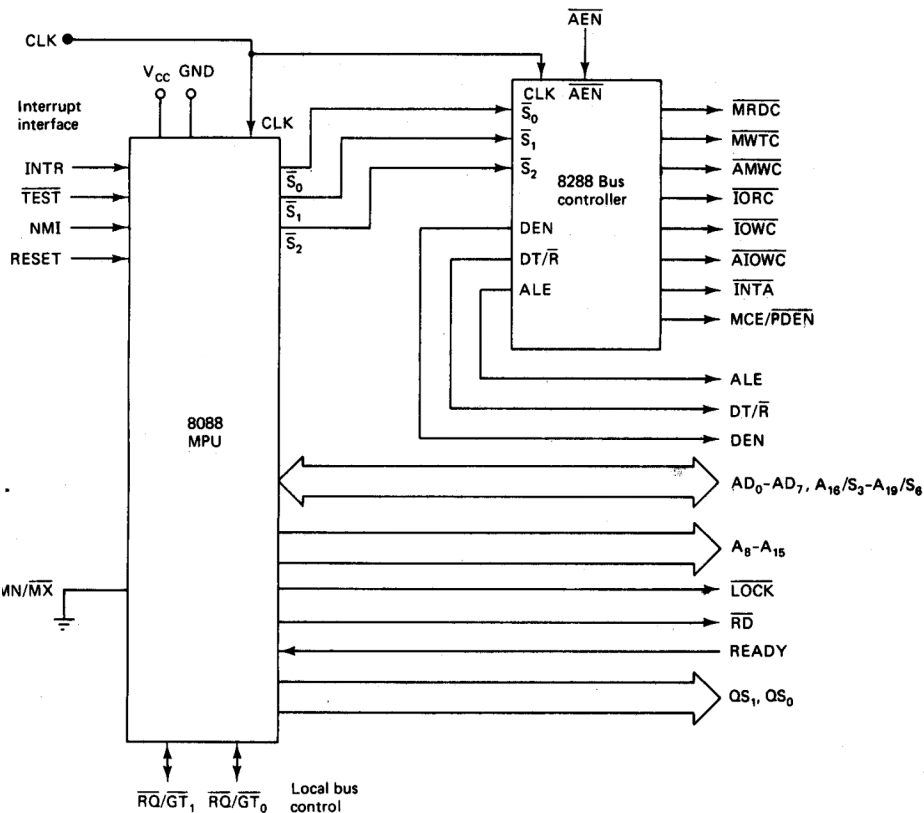
8.4 Maximum-Mode Interfaces– 8088 Interface

- 8288 bus controller connection
  - Inputs are codes from the 3-bit bus status lines
    - S2*S1*S0* = bus status code
  - Outputs produced by 8288 instead of 8088
    - Based on bus status code→ active 0
      - MRDC*= Memory read command
      - MWTC*= Memory write command
      - AMWC*= Advanced memory write command
      - IORC*= I/O read command
      - IOWC*= I/O write command
      - AIOWC*= advanced I/O write command
    - Produced for all bus cycles
      - ALE= Address latch enable
      - DT/R*= Data transmit/receive
      - DEN= Data enable (complement)
      - INTA*= Interrupt acknowledge
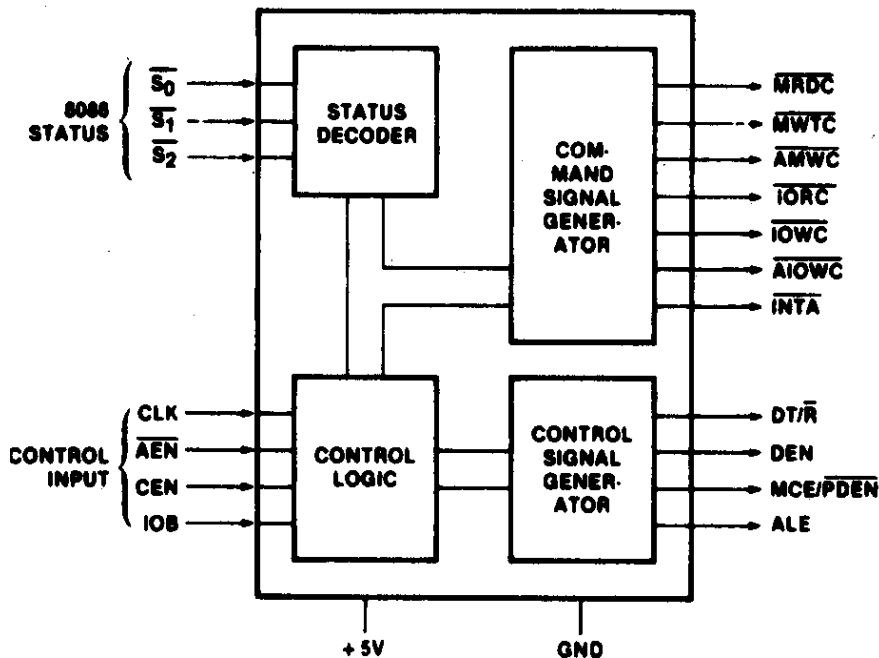
8.4 Maximum-Mode Interfaces– 8088 Interface

Status Inputs			CPU Cycle	8288 Command
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$		
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction Fetch	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

- Bus status codes, associated cycles, and outputs
  - 8088 outputs a bus status code associated with the type of bus cycle to be performed
    - Memory read
    - Memory write
    - Instruction fetch
    - Read I/O port (Input)
    - Write I/O port (Output)
    - Interrupt acknowledge
    - Halt
  - One or two command outputs become active
    - 101 = Memory read → MRDC*
    - 010 = Output → IOWC* and AIOWC*
  - Appropriate signals are connected to drive external memory, IO, and interrupt circuitry

8.4 Maximum-Mode Interfaces– 8086 Interface

- Differences from 8088 maximum-mode interface
  - 16-bit multiplexed data bus
  - BHE* output
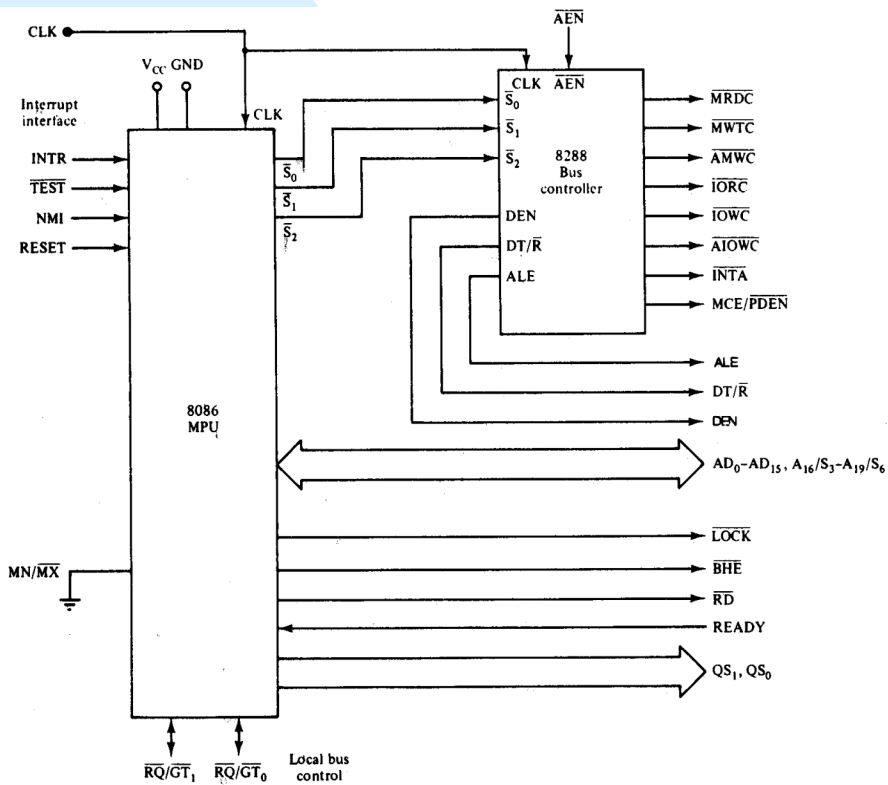
8.5 Electrical Characteristics– Power Supply Ratings and Input/Output Logic Levels

Symbol	Meaning	Minimum	Maximum	Test condition
V_{IL}	Input low voltage	−0.5 V	+0.8 V	
V_{IH}	Input high voltage	+2.0 V	V_{cc} + 0.5 V	
V_{OL}	Output low voltage		+0.45 V	I_{OL} = 2.0mA
V_{OH}	Output high voltage	+2.4 V		I_{OH} = −400 uA

- **Power supply voltages**
  - **Applied between +Vcc and GND**
    - **Vcc= +5V ± 10%**
    - **Icc = 340mA @ 25ºC Output logic levels**
- **Input logic levels—min/max**

  $-.5V \leq V_{IL} \leq +0.8V$

  $+2.0V \leq V_{IH} \leq Vcc+.05V$

- **Output logic levels**

  $V_{OHmin}= +2.4V @ IOH = -400uA$

  $V_{OLmax}= +0.45V @ IOL = 2.0mA*$

  * **Measured at 2.5mA for 8086**

8.6 System Clock– 8284 Clock Generator and CLK
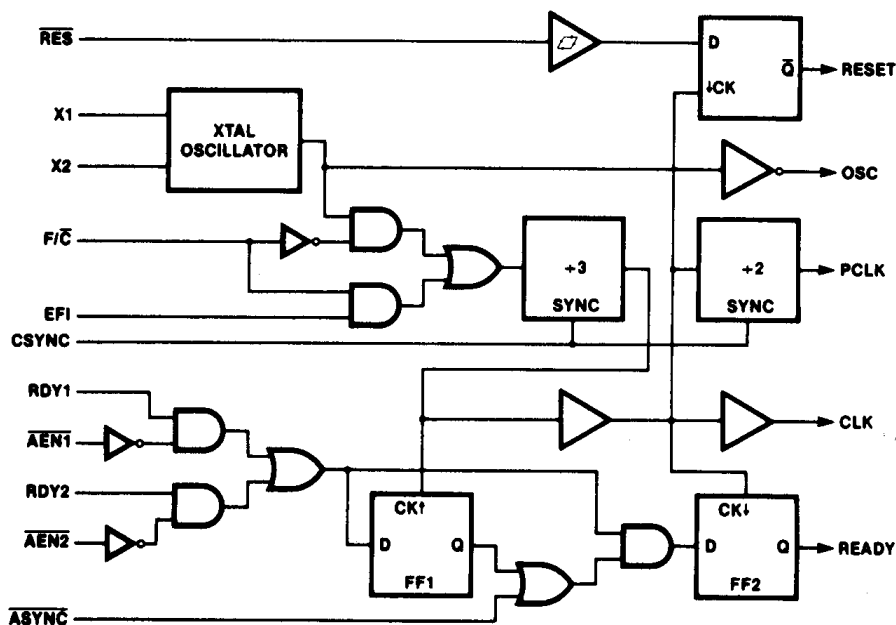
- CLK is used as the time base for synchronization of internal and external operations of the microprocessor and microcomputer

- Standard Clock (CLK) rates of 8008/8086

  - 8088 → 5MHz
  - 8088-2 → 8MHz
  - 8086 → 5MHz
  - 8086-2 → 8MHz
  - 8086-1 → 10MHz

- Other clock outputs

  - PCLK = peripheral clock = ½ X CLK
  - OSC = oscillator clock = 3 X CLK

- Other functions of 8284

  - Reset synchronization
  - Ready synchronization

8.6 System Clock– 8284 to 8088 Connection

- Crystal between X1 and X2 pins of 8284
  - Fundamental frequency is 3X CLK

    15MHz for 5MHz 8088

    24MHz for 8 MHz 8088
- F/C* selects the clock source

  0 = crystal attached to X1 and X1

  1 = external clock at EFI input
- CLK output is at MOS levels, but attaches directly to CLK input of 8088
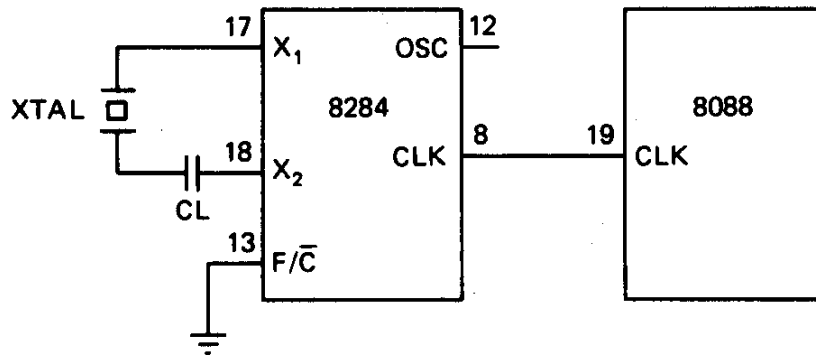
8.7 Bus Cycles and Time States– Types of Bus Cycles
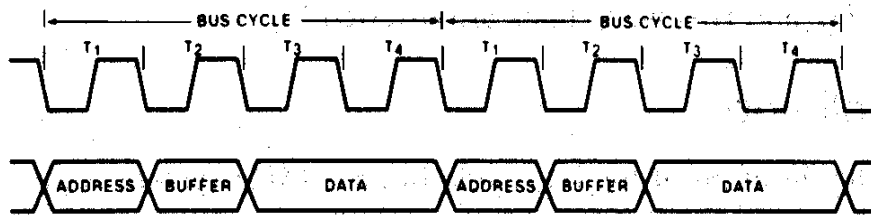
- Bus cycle is the operation performed by the microprocessor to access an external device
  - Memory read bus cycle
  - Memory write bus cycle
  - IO read (input) bus cycle
  - IO write (output) bus cycle
- Duration and states of the bus cycle
  - 4 clock cycles per bus cycle
  - Time states called T1, T2, T3, T4
  - At 8MHZ T state = 125ns and bus cycle duration is 500ns
- Multiplexed address/data transfer operation
  - Address output during T1
  - Bus lines in high-Z state in T2
  - Data transfer takes place during states T3 and T4

8.7 Bus Cycles and Time States– Idle and Wait States
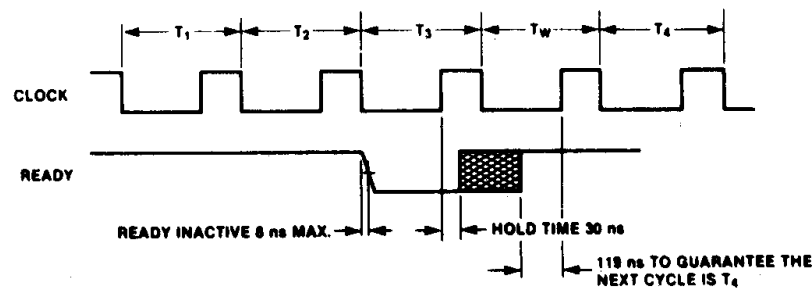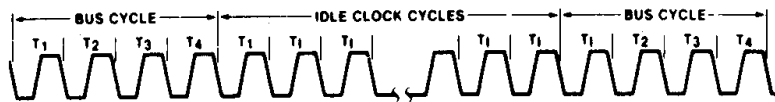
- Bus cycle with idle
  - If no bus activity is necessary, microprocessor inserts idle states between bus cycles
  - Identified as Ti
  - May be due to the fact that the instruction queue is already full so no instructions need to be fetched
- Bus cycle with wait states
  - If the memory or I/O device is not able to respond in the duration of a bus cycle (500ns @8MHz), it must make READY 0 during T3 to extend the bus cycle
  - Wait states (Tw) are inserted to extend the bus cycle until READY returns to 1
  - 8MHz bus cycle with 2 wait state = 750ns

Introduction

8.8 Hardware Organization of the Memory Address Space– 8088 Microprocessor

1M BYTES

FFFFF

FFFFE

2

1

0

$A_{19}-A_0$ D_7-D_0
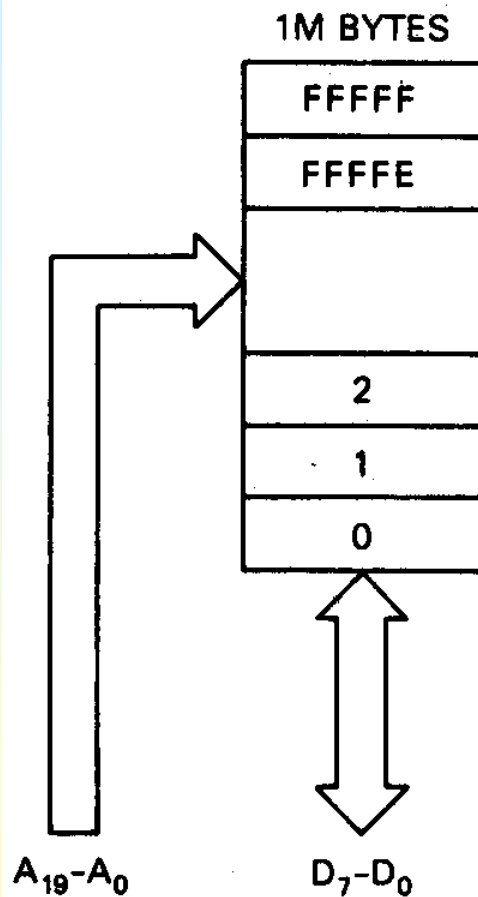
- 8088 memory hardware is organized as a single byte-wide memory bank
  - Size—1M X 8 bits
  - Physical address range— 0H–FFFFFH
  - Address/data bus demultiplexed in external hardware
  - Input:
    20-bit address bus— A19 through A0
  - Input/Output:
    8-bit data bus—D7 Through D0

8.8 Hardware Organization of the Memory Address Space– 8088 Memory Accesses

Transfer X

X + 1

(X)

A₁₉-A₀   D₇-D₀

(a)

First bus cycle

X + 1

(X)

A₁₉-A₀   D₇-D₀

Second bus cycle

(X + 1)

X

A₁₉-A₀   D₇-D₀

(b)

- ▪ Byte access bus cycle
    - MPU applies address of storage location to be accessed over address lines A19-A0
        - A19—most significant bit
        - A0—least significant bit
    - Byte of data written into or read from address X transferred over data lines D0 through D7
        - D7—most significant bit
        - D0—least significant bit
    - Byte access takes a minimum of one bus cycle of duration
        - @5MHz—800ns
        - @8MHz—500ns
- ▪ Word access bus cycles
    - MPU must access two consecutive storage locations in memory—X and X+1
    - Requires two bus cycles
        - Address X accessed during cycle 1
        - Address X+1 accessed during cycle 2
    - Word access duration is a minimum of two bus cycle
        - @5MHz—2 X 800ns = 1600ns
        - @8MHz—2 X 500ns = 1000ns
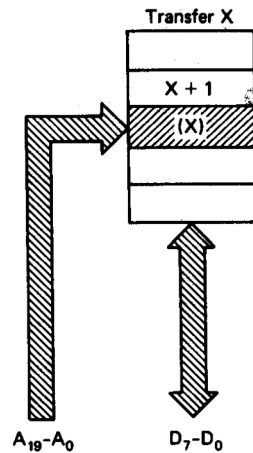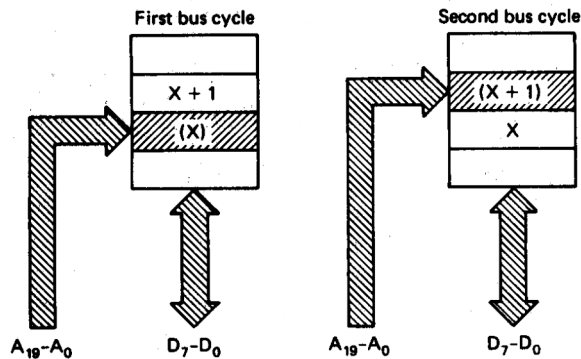
8.8 Hardware Organization of the Memory Address Space– 8086 Microprocessor

- 8086 memory hardware is organized as a two byte-wide memory bank
  - Bank size—512K X 8 bits
    - Low-bank holds even addressed bytes—0H through FFFFEH
    - High-bank holds odd addressed bytes—1H through FFFFFH
  - Address/data bus demultiplexed in external hardware
  - Input:
    20-bit+ address bus— A19 through A0, and BHE*
      A1-A19 = selects storage location
      A0 = 0 enables low bank
      BHE* = 0 enables high bank
  - Input/Output:
    16-bit data bus—D15 Through D0
        D7-D0 $\rightarrow$ even addressed byte accesses
        D15-D8 $\rightarrow$ odd addressed byte accesses
        D15-D0 $\rightarrow$ word accesses
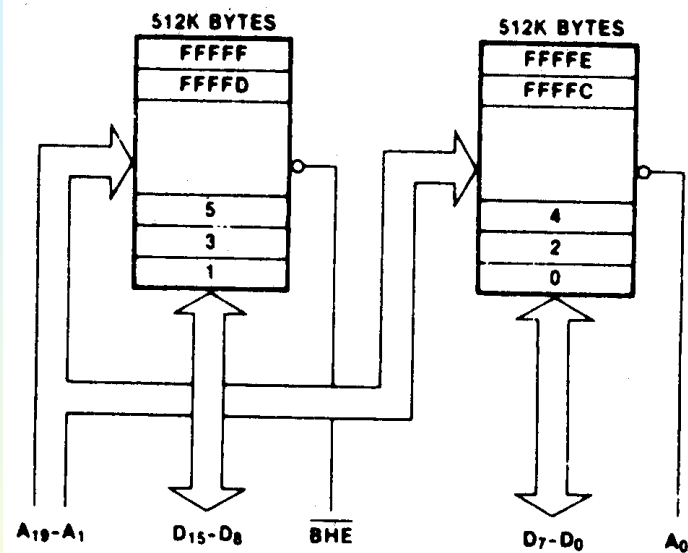
8.8 Hardware Organization of the Memory Address Space– 8086 Aligned Memory Accesses
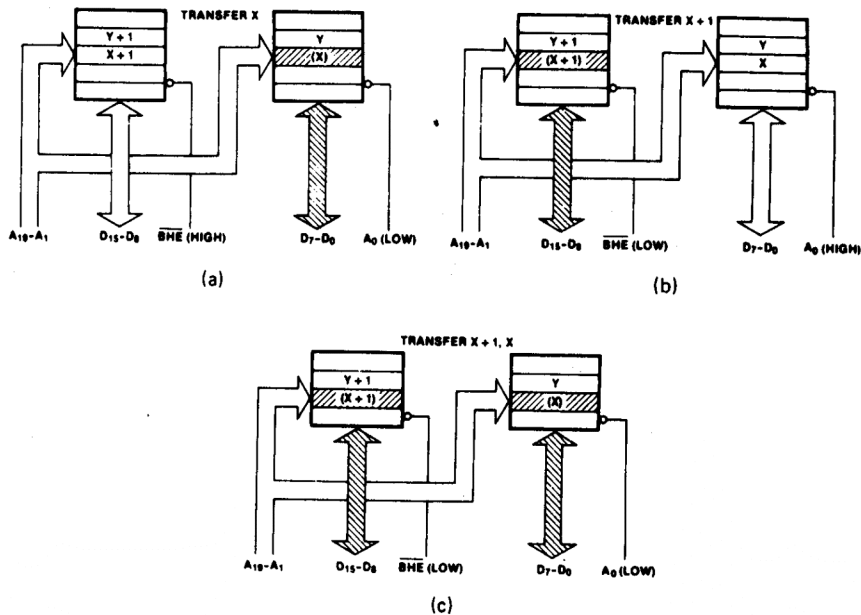
- Low bank byte access bus cycle
  - MPU applies even address X to both banks over address lines A19-A0
  - MPU enables just the low bank

    BHE*A0 = 10 → enables low bank
  - Byte of data written into or read from address X transferred over data lines D0 through D7
- High bank access bus cycle differences
  - **Odd address X+1 applied to both banks**
  - **High bank enabled**

    BHE*A0 =01 = → enable high bank
  - **Byte-wide data transfer takes place over data line D8 through D15**
- Word access bus cycle differences
  - **Even word address X applied to both banks**
  - **MPU enables both banks**

    BHE*A0 =00 = → enable low and high bank
  - **Word-wide data transfer takes place over D0 through D15**
- All accesses takes a minimum of one bus cycle of duration

    @5MHz—800ns

    @8MHz—500ns

FIRST BUS CYCLE

x + 3
(x + 1)

x + 2
x

A₁₉-A₁   D₁₅-D₈   BHE (LOW)   D₇-D₀   A₀ (HIGH)

SECOND BUS CYCLE

x + 3
x + 1

x + 2
x

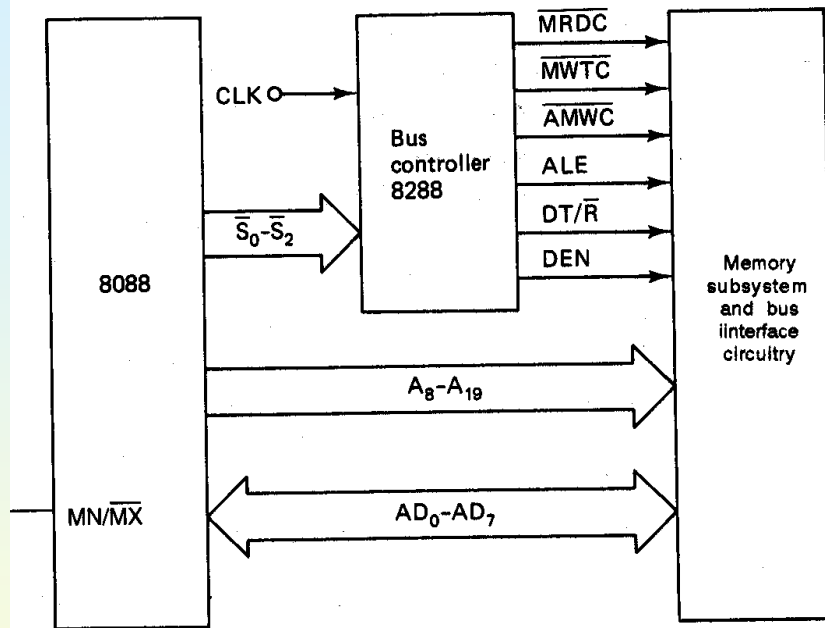A₁₉-A₁   D₁₅-D₈   BHE (HIGH)   D₇-D₀   A₀(LOW)
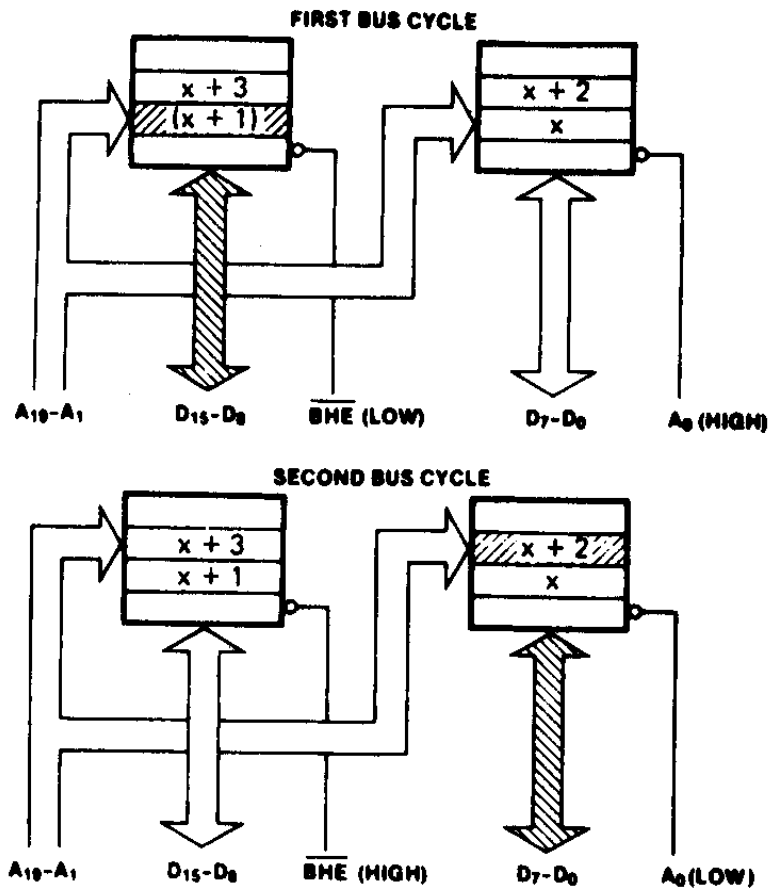
(d)

- **Misaligned-word access bus cycles**
  - **Word starting at address X+1 is misaligned**
  - **Requires two bus cycles**
    - **Access byte at address X+1 during cycle 1**
      A19-A0 = X+1
      BHE*A0 =01→ enables high bank
      D15-D8 → carries data
    - **Access byte at address X+2 during cycle 2**
      A19-A0 = X+2
      BHE*A0 =10→ enables low bank
      D7-D0 → carries data
  - **Word access duration is a minimum of two bus cycle**
    @5MHz—2 X 800ns = 1600ns
    @8MHz—2 X 500ns = 1000ns
  - **Impact on performance—software should minimize accessing misaligned data**

8.10 Memory Control Signals– 8088
Minimum-Mode Interface

- Multiplexed-address data bus
    - AD0-AD7
    - A8-A19
- Control signal review
    - ALE = pulse to logic 1 tells bus interface circuitry to latch address
    - RD* = logic 0 tells memory subsystem that a code or data read is in progress
    - WR*= logic 0 tells memory subsystem that a data write is in progress
    - IO/M*= Logic 0 tells interface circuits that the data transfer operation is for the memory subsystem
    - DT/R* = sets the direction of the external data bus for read(input) or write(output) operation
    - DEN*= enables the interface between the memory subsystem and MPU data bus
    - SSO* = tells memory interface whether the memory access is a code read or data access

- **Maximum-mode interface differences review**
  - **8288 bus controller produces the control signals**
  - **Signal changes**
    - **MRDC* replaces RD***
    - **MWTC* and AMWC* replace WR***
    - **DEN is complement of DEN***
    - **IO/M* no longer needed (bus controller creates separate memory and IO read/write controls)**
    - **SSO* no longer part of interface**

8.10 Memory Control Signals– 8088
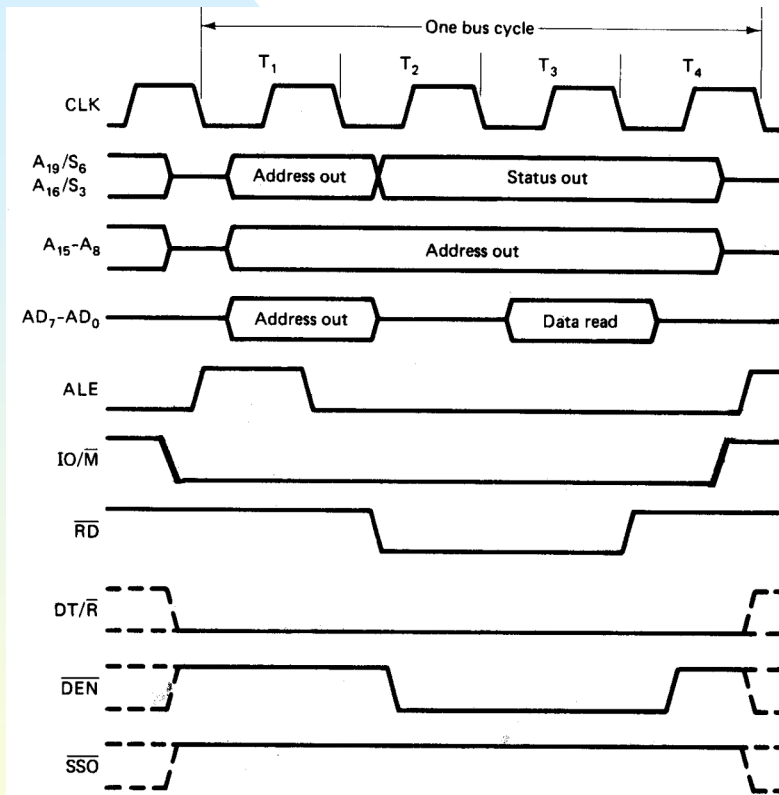## Maximum-Mode Interface

Status Inputs			CPU Cycle	8288 Command
$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$		
0	0	0	Interrupt acknowledge	$\overline{INTA}$
0	0	1	Read I/O port	$\overline{IORC}$
0	1	0	Write I/O port	$\overline{IOWC}, \overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction fetch	$\overline{MRDC}$
1	0	1	Read memory	$\overline{MRDC}$
1	1	0	Write memory	$\overline{MWTC}, \overline{AMWC}$
1	1	1	Passive	None

- Memory bus status code review
  - During all memory accesses one of three bus cycle status code are output by the MPU
    - Instruction fetch
    - Read memory
    - Write memory
  - 8288 decodes to produce appropriate control command signals
    - MRDC* → instruction fetch/memory read
    - MWTC* → memory write
   - AMWC* → advanced memory write

- Read bus cycle timing diagram—shows relationship between signals relative to times states
  - **T1 state—read cycle begins**
    - Address output on A0-A19
    - Pulse produced at ALE--address should be latched in external circuitry on trailing edge of ALE
    - IO/M* set to 0→ memory bus cycle
    - DT/R* set to 0→ set external data bus control circuitry for receive mode (read)
  - **T2 state**
    - Status code output on S3-S6
    - AD0 through AD7 tri-stated in preparation for data bus operation
    - RD* set to 0→ read cycle
    - DEN* set to 0 → enable external data bus control circuitry
  - **T3 state**
    - Data on D0-D7 read by the MPU
  - **T4 state—read cycle finishes**
    - RD* returns to 1→ inactive level
    - Complete address/data bus tri-stated
    - IO/M* returned to 1 → IO bus cycle
    - DEN* returned to 1→ inactive level
    - DT/R* returns to 1→ transmit level

Minimum Mode Read Bus Cycle
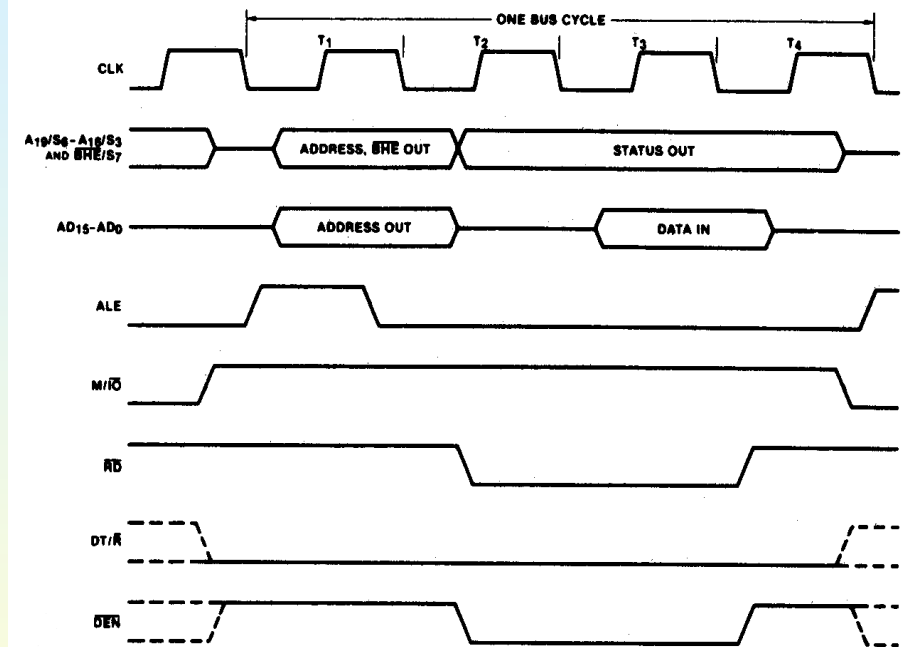
- Differences of 8086 read bus cycle
  - BHE* is output along with the address in T1
  - Data read by the MPU can be carried over all 16 data bus lines
  - M/IO*—which replaces IO/M*—switches to 1 instead of 0 at the beginning of T1
  - SSO* signals is not produce

Minimum Mode Write Bus Cycle

- Write bus cycle timing diagram—shows relationship between signals relative to times states
  - **T1 state—write cycle begins**
    - Address output on A0-A19
    - Pulse produced at ALE and address latched in external circuitry on trailing edge of ALE
    - IO/M* set to 0→ memory bus cycle
    - DT/R* remains at 1→ external data bus control circuitry for transmit mode (write)
  - **T2 state**
    - Status code output on S3-S6
    - AD0 through AD7 transitioned to data bus and write data placed on bus
    - DEN* set to 0 → enable external data bus control circuitry
    - WR* set to 0→ write cycle
  - **T3 or T4 state**
    - Data on D0-D7 written into memory (memory decides when!)
  - **T4 state—write cycle finishes**
    - WR* returns to 1→ inactive level
    - Complete address/data bus tri-stated
    - IO/M* returned to 1 → IO bus cycle
    - DEN* returned to 1→ inactive level
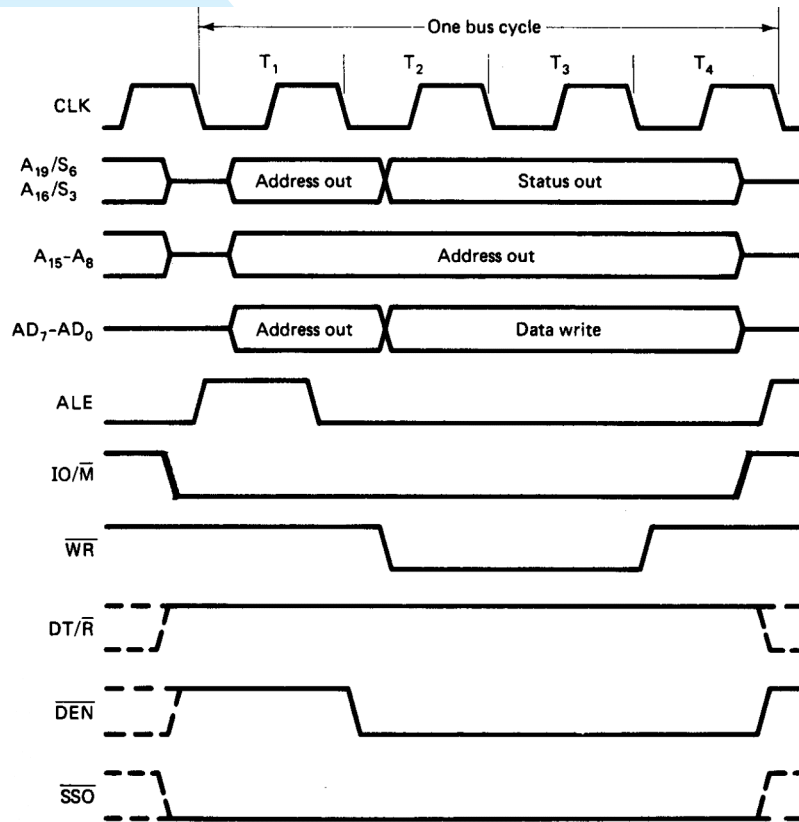
8.11 Read and Write Bus Cycles– 8086
## Maximum Mode Write Bus Cycle
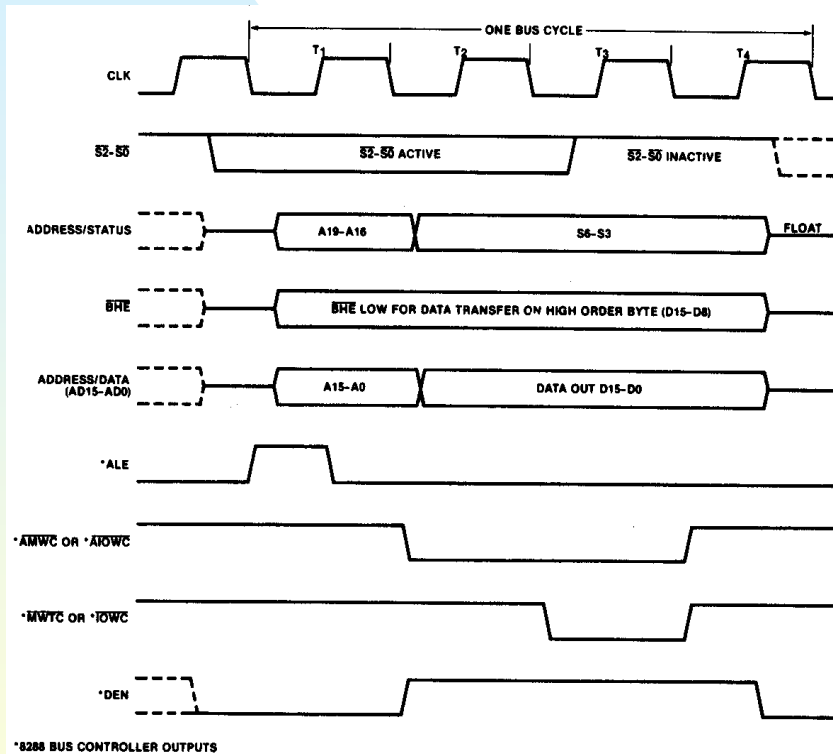
- Similar to 8088/8086 minimum-mode write bus cycle
  - Address and data transfer operation identical
  - Transfer may be a high-byte, low-byte, word
- Differences is the 8288 produces the bus control signals—ALE, DEN, AMWC*, and MWTC*
  - Bus status code S2*-S0* output prior to T1 and held through T2
  - AMWC* and MWTC* replace WR* (Note timing difference)
  - DEN =1 produced instead of DEN* =0 (change in external circuitry!)

8.12 Memory Interface Circuits– **Block Diagram**

- Building blocks of the maximum mode 8086 memory interface
  - 8288 bus controller
  - Address bus latch
  - Address decoder
  - Data bus transceiver/buffer
  - Bank read control logic
 - Bank write control logic
  - Memory subsystem
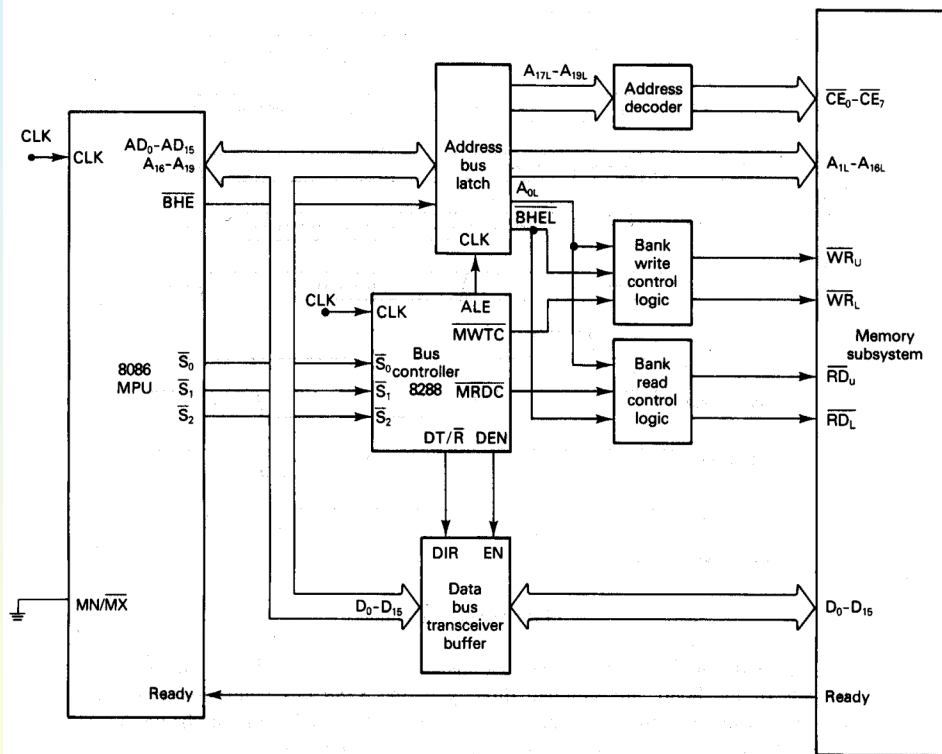
8.12 Memory Interface Circuits– Overview of Memory Access Operation

- **Overview of the memory access**
  - Bus status code for type of memory access output to 8288 on S2*-S0*
  - 8288 decodes to produce the command and control signals need to coordinate the data transfer
  - Address is latched, buffered, and decoded to:
    - Produce chip enable signals for the memory array
    - Select a specific memory location
    - Select upper, lower, or both banks of the memory array
  - MWTC* and MRDC* combined with A0L and BHEL* to set the appropriate bank(s) of the memory array for write or read, respectively
  - DT/R* and DEN are used to enable the data bus transceiver/buffer and set it for the transmit (write) or receive (read) direction
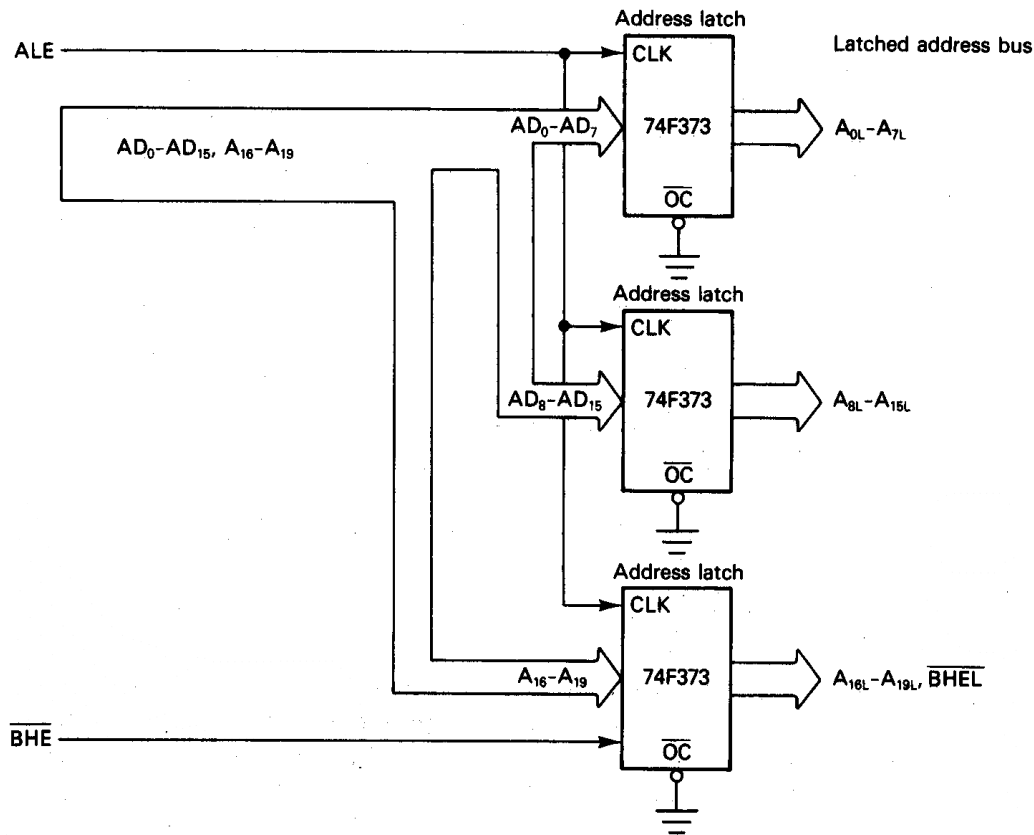
8.12 Memory Interface Circuits– Address Latch

(a)

(b)
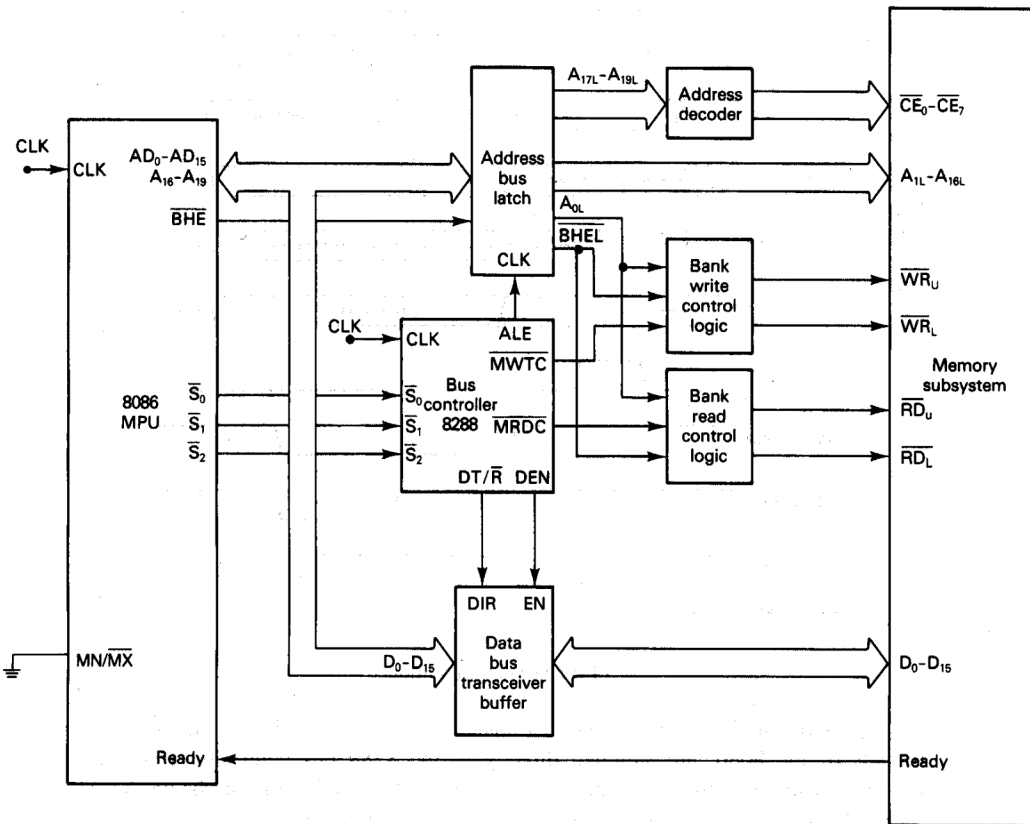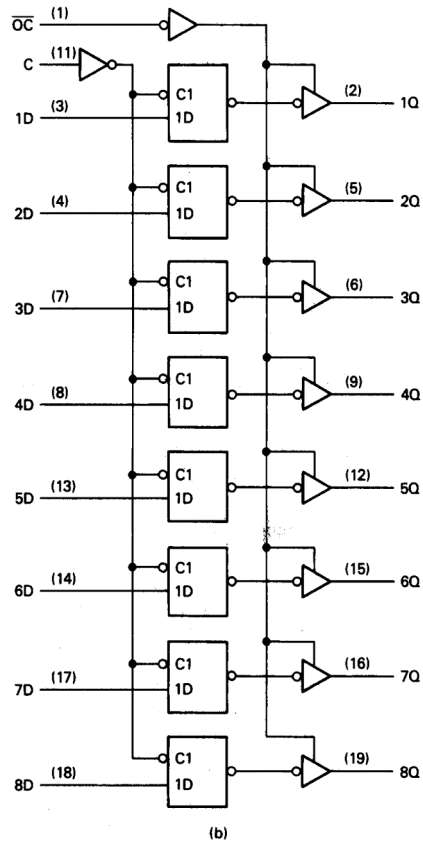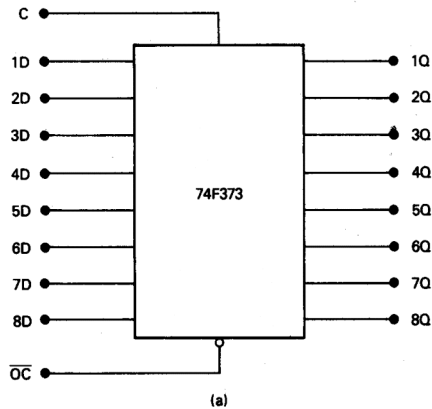
Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_o
H	X	X	Z

(c)

- Roles of the address latch
  - Latch address signals A0-A19 and BHE*
  - Buffer signals so that they may be used to drive a large memory system, IO peripherals, and other interfaces
- Requirements
  - 21 bit wide latch/buffer
  - Low propagation delay– allows use of slower memories
- 74F373—Octal D-type latch
  - 8 independent buffered D-type flip-flops (latches)
  - Enable to output propagation delay = 13 ns
  - Outputs sink 24 mA (buffering)
  - OC* =0 enables latch circuits

8.12 Memory Interface Circuits– Address Latch Design


- Implemented with 3 74F373 Octal-D-type latches
  - Inputs AD0-AD15, A16-A19, and BHE* from MPU
  - All devices permanently enabled by fixing the OC* inputs at logic 0
  - All latches clocked in parallel with pulse at ALE from 8288
  - Latched and buffered outputs are: A0L-A19L, and BHEL*
  - Parts of address applied to the address inputs of memory subsystem, address decoder, and read/write control logic

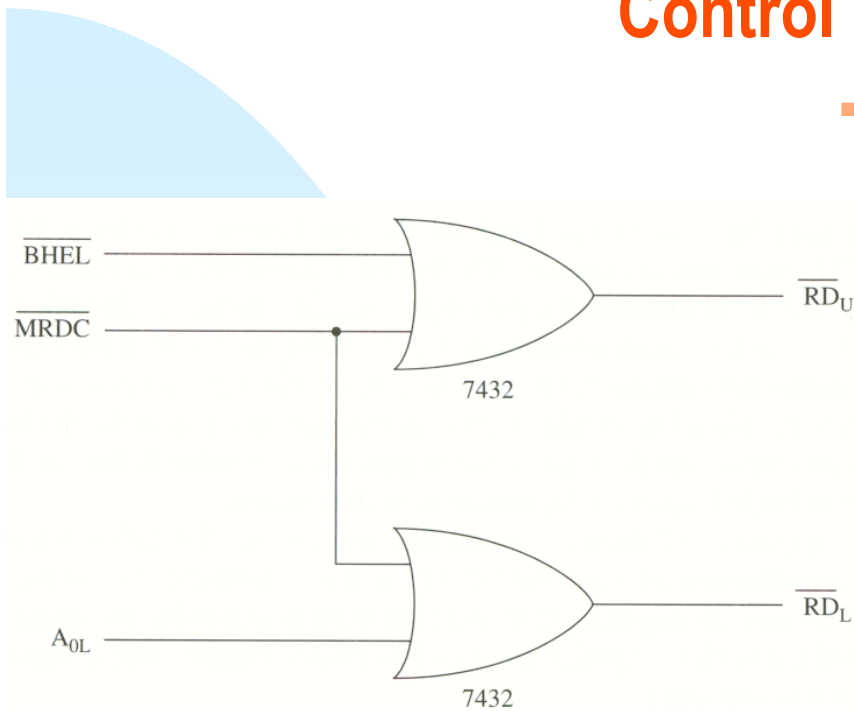# 8.12 Memory Interface Circuits– Bank Write Control Logic Design

- ▪ Role of write control logic
  - • Memory array is organized in upper and lower banks
  - • Types of data writes that may take place:
    - • Byte to a storage location in the upper (odd) bank
    - • Byte to a storage location in the lower (even) bank
    - • Word to storage locations in both banks
  - • Write control logic must decode A0L, BHEL*, and MWTC* to produce independent write signals—WR_U* and WR_L*
  - • 7432—2-input OR gate solution
    - • MWTC*(MWRC*) =0 enables both gates

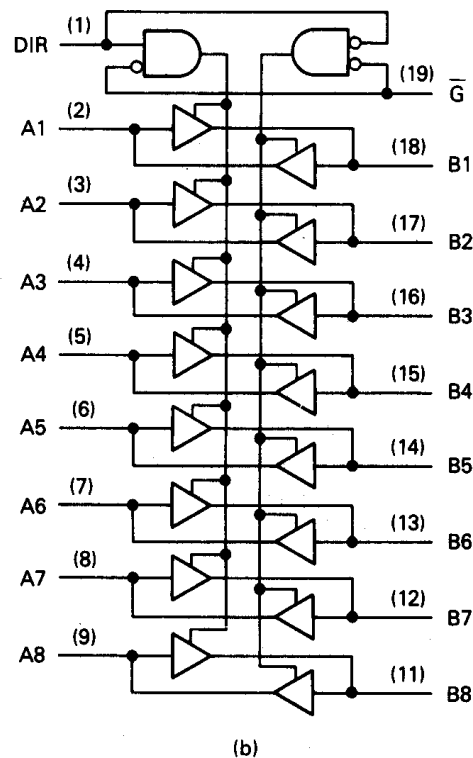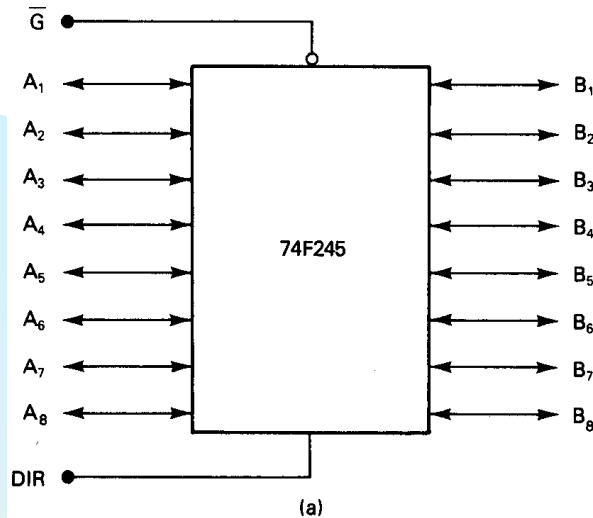| BHEL*	AOL	WR_U*	WR_L*	Result
0	0	0	0	Both banks enabled
1	0	1	0	Lower (even) bank enabled
0	1	0	1	Upper (odd) bank enabled
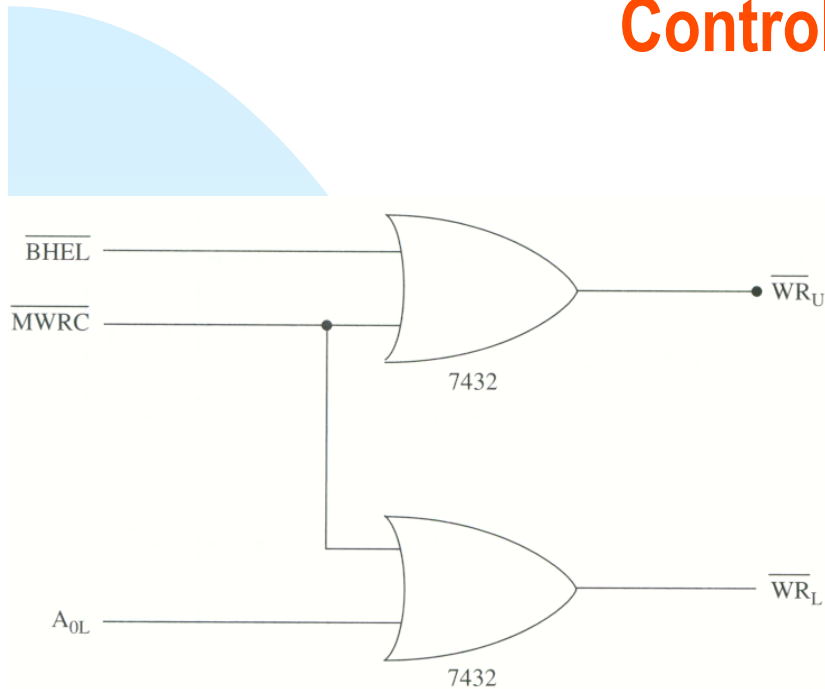
8.12 Memory Interface Circuits– Bank Read Control Logic Design

- Role of read control logic
  - Types of data reads that may take place:
    - Byte from the lower (even) bank
    - Byte from upper (odd) bank
    - Word of data from both banks or an instruction fetch
  - Read control logic must decode A0L, BHEL*, and MRDC* to produce independent read signals—RD_U* and RD_L*
  - 7432-based solution is similar to bank write control logic
    - MRDC* =0 enables both gates

BHEL*	AOL	RD_U*	RD_L*	Result
0	0	0	0	Both banks enabled
1	0	1	0	Lower (even) bank enabled
0	1	0	1	Upper (odd) bank enabled

(a)

(b)
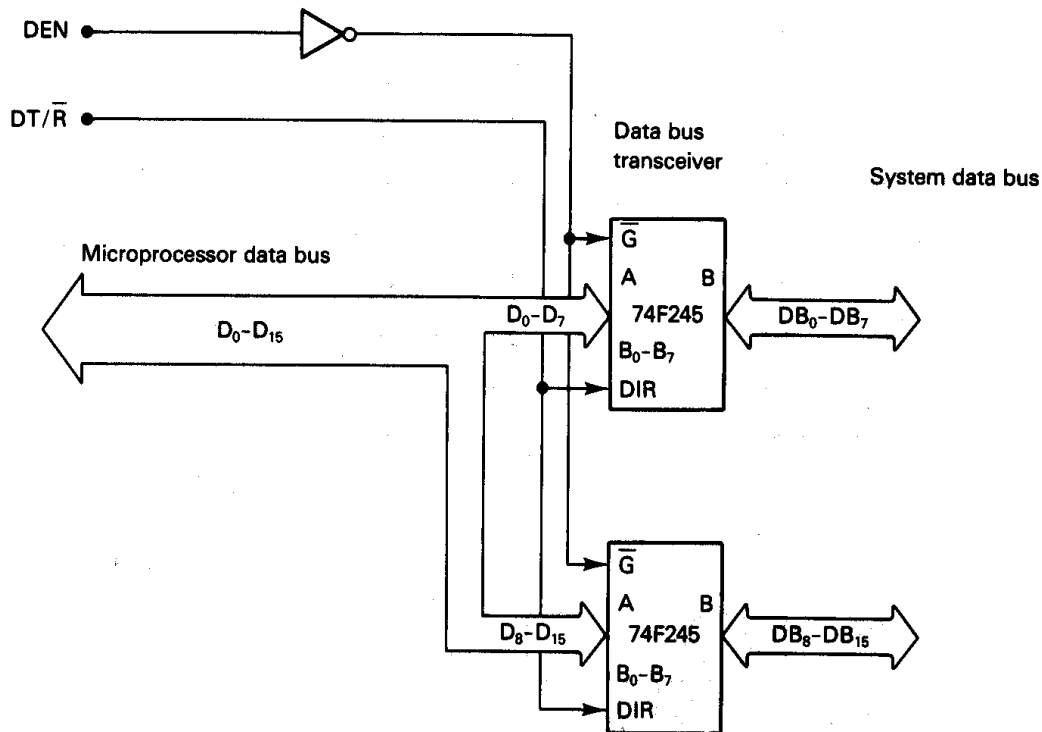
8.12 Memory Interface Circuits– Data Bus Transceivers

- Roles of the data bus transceiver/buffer
  - Set the direction of the data path been memory and the MPU bus
  - Appropriately time the enabling of the transceivers to coincide with the read/write data transfer
  - Buffer the data bus lines so that they may be used to drive a large memory system, IO peripherals, and other interfaces
- Requirements
  - 8/16 bit wide bi-directional transceiver
  - Low propagation delay– allows use of slower memories
- 74F245—Octal bi-directional bus transceiver
  - 8 independent bus transceivers
  - DIR input selects direction of data transfer
    - 0 = B to A → read
    - 1 = A to B → write
  - G* =0 enables all transceivers
  - Outputs sink 64 mA (buffering)

8.12 Memory Interface Circuits– Data Bus Transceiver Design

DEN

DT/$\overline{R}$

Data bus transceiver

System data bus

Microprocessor data bus

D_0-D_{15}

D_0-D_7

$\overline{G}$

A   B

74F245

B_0-B_7

DIR

DB_0-DB_7

D_8-D_{15}

$\overline{G}$

A   B

74F245

B_0-B_7

DIR

DB_8-DB_{15}

- Implemented with 2 74F245 Octal bi-directional bus transceivers
  - A inputs/outputs are D0-D15 directly from MPU
  - Direction of both devices set by logic level of DT/R*
  - Both devices enabled at appropriate time for data transfer by DEN=1
  - B inputs/outputs are the buffered data bus lines DB0 through DB15
  - Buffered data bus lines applied directly to the memory subsystem

# 8.12 Memory Interface Circuits– Address bus with Latch and Decoder
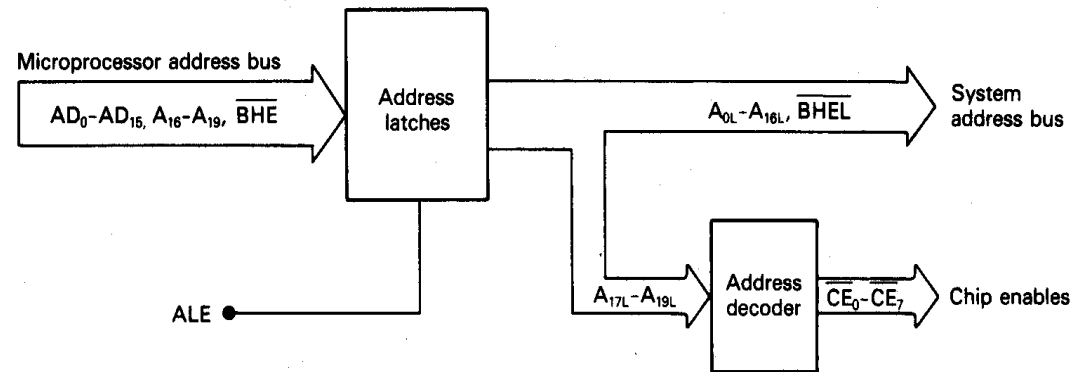
- Role of address decoder
  - Part of the buffered/latched address is decoded to create chip enables
    - Address inputs A19L A18L A17L is decoded to produce 8 independent chip enable outputs CE0* through CE7*
    - Inputs and outputs

A19L	A18L	A17L	CE0*	CE1*	CE2*	CE3*	CE4*	CE5*	CE6*	CE7*
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

  - Byte from the lower bank

8.12 Memory Interface Circuits– Address Decoder
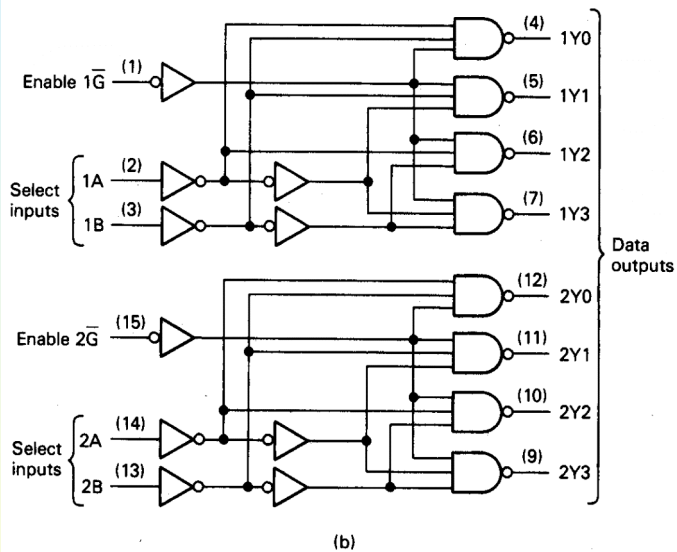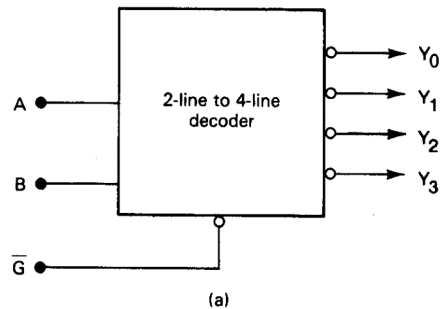


(a)

(b)

(c)

- Requirements of Address Decoder
  - Requires standard decoder/multiplexer functions
    - 2-input 4-output—74F139
    - 3-input 8-output—74F138
  - 74F139 decoder/multiplexer
    - Dual 2-input 4-output decoder/multiplexer
      - Two-bit input BA
      - Four independent outputs Y0 through Y3
      - G* input enables the associated decoder
  - Operation
    - G* = 1 forces all outputs to 1
    - G* = 0 enables circuit and the Y output associated with the input code switches to the active 0 level

# 8.12 Memory Interface Circuits– 3-input 8-Output Address Decoder Design Using the 74F139
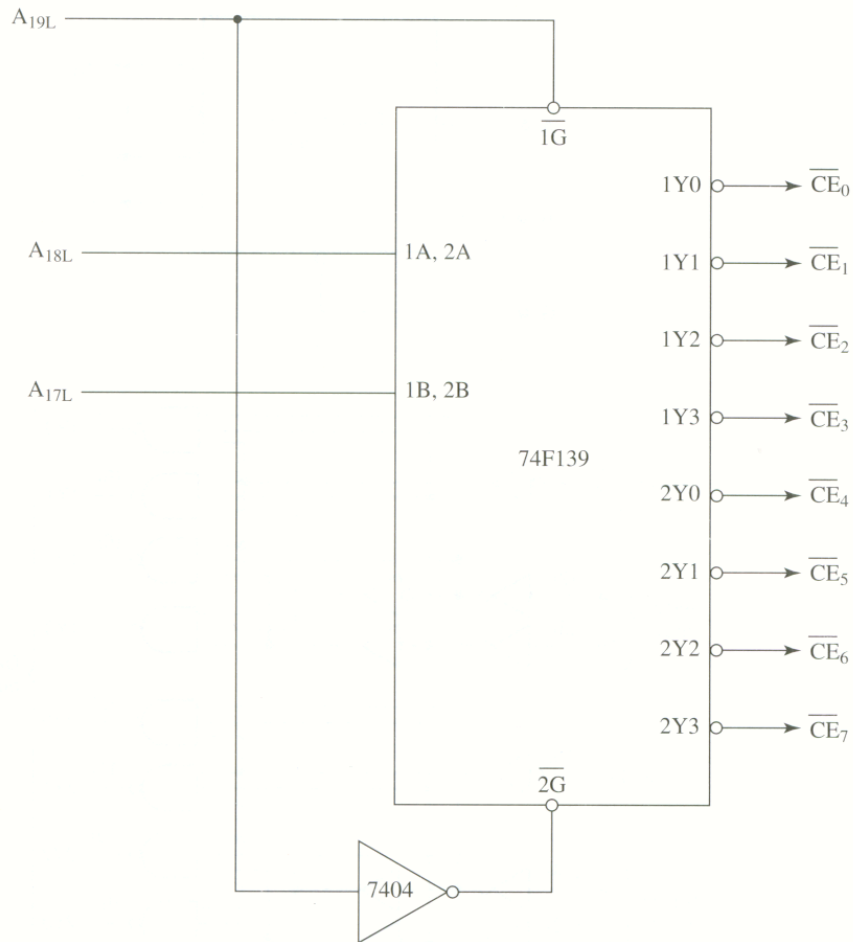
- 3-input 8-output address decoder made with two 2-input 4-output decoder/multiplexer circuits
  - A19L =0 makes 1G* =0 and 2G* =1 and enables outputs CE0*-CE3*
  - A19L =1 makes 1G* =1 and 2G* =0 and enables CE4*-CE7*
  - Code at A18L A17L applied to the BA inputs of both multiplexers in parallel
  - Output associated with the input code on the enabled decoder becomes active

8.12 Memory Interface Circuits– 3-Input 8-Output Address Decoder Design Using the 74F138
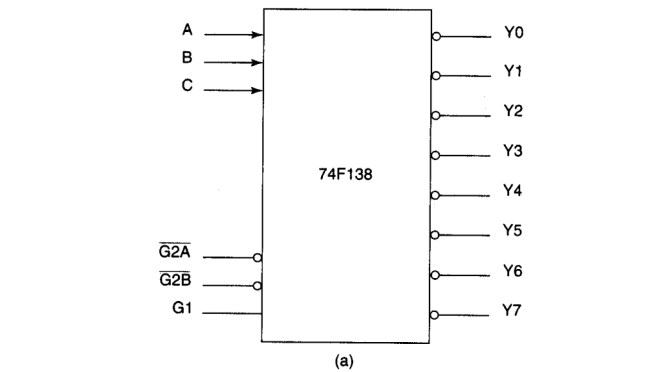
(a)
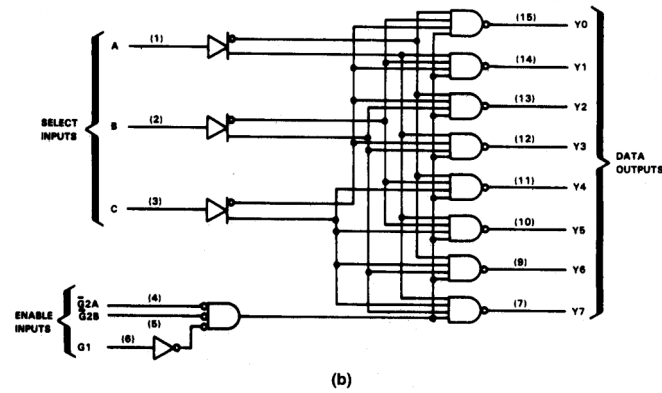
(b)

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

(c)