

## CHAPTER 9

# LATCHES AND FLIP-FLOPS

### 9.1 Introduction

All the logic circuits studied thus far are combinational circuits. The outputs of a combinational circuit depend on the inputs at the time of measurement. In other words, a combination of logic values at the inputs will determine the logic values at the outputs after the circuit becomes stable. For a sequential circuit, the outputs depend not only on the inputs at the time of measurement but also on the inputs applied to the circuit in the past. Therefore the outputs of a sequential circuit depend on a "sequence" of inputs and the order the inputs are applied to the circuit.

The structure of a sequential circuit is shown in Figure 9.1. In order to "memorize" what inputs have been fed to the circuit in the past, a memory is included in a sequential circuit. The memory may not memorize the exact past inputs. Instead, they are transformed into information representing a certain condition of past inputs, which is called a state. Transformation of past inputs is carried out by a combinational circuit. Inputs to a memory are called excitations. Outputs of a memory are called states. The combinational circuit is used to produce the excitations as well as the outputs of the sequential circuit.

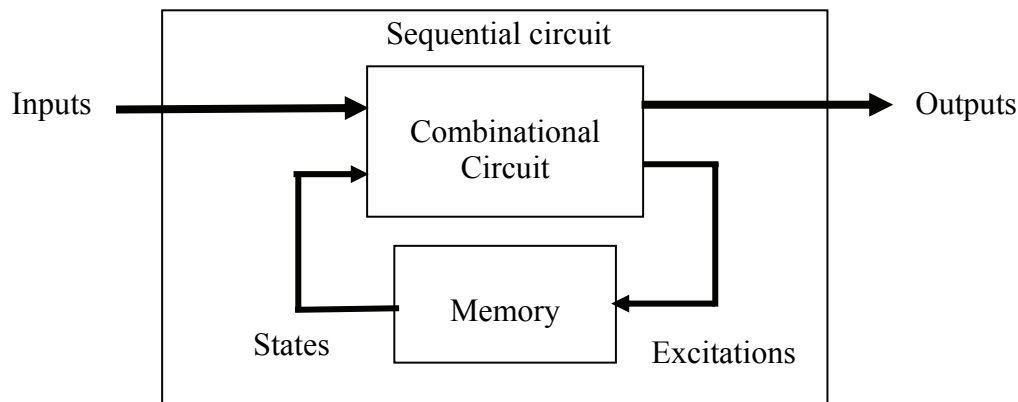


Figure 9.1 Structure of a sequential circuit.

There are two types of sequential circuits: synchronous and asynchronous. A memory element in a synchronous sequential circuit is called a flip-flop. A flip-flop can store one bit of information. The flip-flops in a synchronous sequential circuit are synchronized and triggered by a clock. As shown in Figure 9.2, the clock generates continuous and periodic pulses. The transition of a clock signal from 0 to 1 is called

positive edge, leading edge, or rising edge. The transition from 1 to 0 is called negative edge, trailing edge, or falling edge. The duration between two successive positive (or negative) edges is called one clock cycle or period. The number of clock pulses generated in one second is called the clock frequency. Clock frequency is the reciprocal of clock period. The excitations will not affect the state until the flip-flops are triggered by the clock. The memory elements in an asynchronous sequential circuit, on the other hand, are not controlled by a clock.

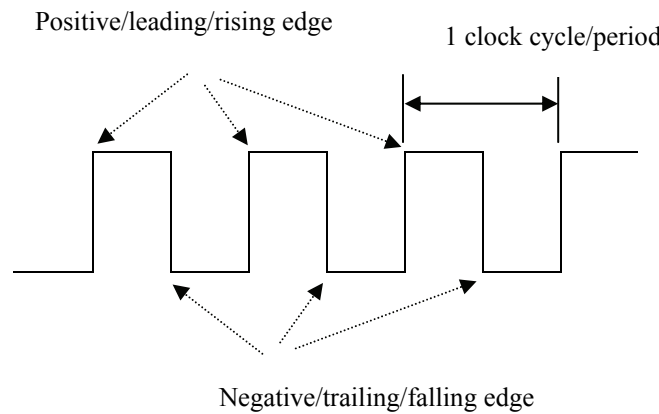


Figure 9.2 Clock for a synchronous sequential circuit.

## 9.2 SR Latch

A SR latch is a memory element that can be used in an asynchronous sequential circuit. Similar to a flip-flop, it can also store one bit of information. A SR latch constructed from two NOR gates is shown in Figure 9.3. Because the output of one NOR gate serves as one of the two inputs to the other NOR gate, it is called a cross-coupled NOR circuit. The information is stored at the output Q. Although there are two outputs, the other output is Q' which does not provide any information beyond what has already been known at Q. Since the two outputs are complements to each other, they should have different values. A latch does not function properly if the logic values of Q and Q' are the same. The two inputs S and R are active-high signals. When S, which denotes "set", is asserted,  $Q = 1$ . When R, which stands for "reset" or sometimes known as "clear", is asserted,  $Q = 0$ . When  $S = R = 0$ , both inputs are not asserted and the both 1 and 0 at the same time. Thus  $S = R = 1$  should be avoided.

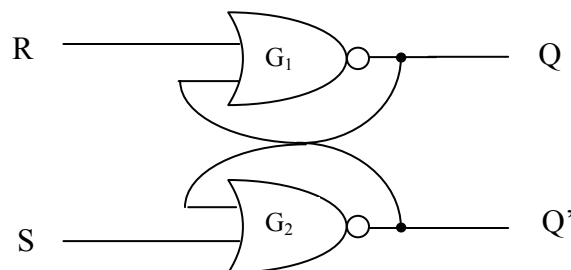


Figure 9.3 A cross-coupled NOR SR latch.

SR latch is itself an asynchronous sequential circuit. For an asynchronous sequential circuit to operate properly, only one input can change at a time. The circuit may not become stable until after some propagation delays through the gates. No input change is allowed until the circuit becomes stable.

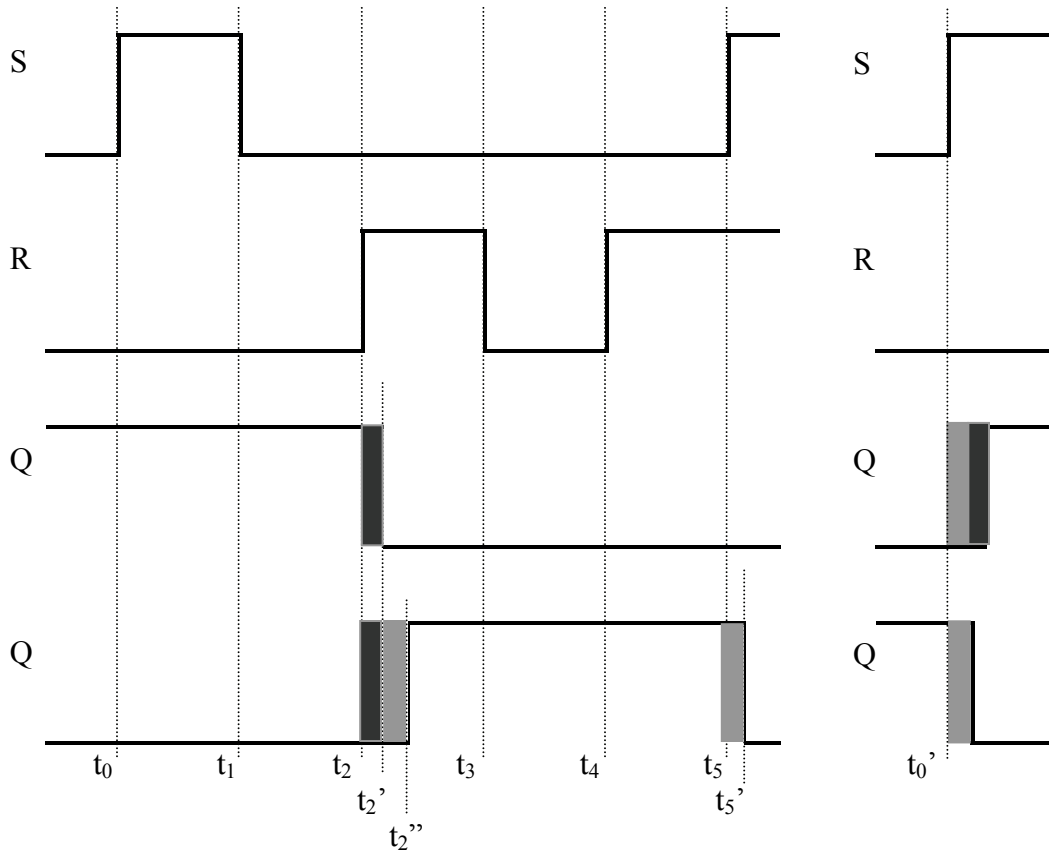


Figure 9.4 Timing diagrams for the cross-coupled NOR SR latch.

The responses at Q and Q' due to changes at S and R are shown by the timing diagrams in Figure 9.4 and listed in a table known as a characteristic table in Table 9.1. In studying the characteristics of latches and flip-flops, present state and next state are used to describe the value of Q due to input changes. At the time an input to a latch changes its value, the values of all inputs are called “present inputs”. The value of Q at the time of and before an input change is called “present state”. The expected value of Q due to the input change is called “next state” and written as  $Q^+$ . As time goes on, next state always becomes present state.

In Figure 9.4, assume  $S = R = 0$ ,  $Q = 1$ , and  $Q' = 0$  in the beginning. At  $t_0$ , the value of S changes from 0 to 1. The present inputs are  $S = 1$ ,  $R = 0$ . The present state is  $Q = 1$ . The change at S does not affect the values of Q and Q'. At the right of Figure 9.4, the value of Q is assumed to be 0,  $Q' = 1$ , and  $S = R = 0$  in the beginning. When the value of S changes to 1 at  $t_0'$ , after the propagation delay in the NOR gate  $G_2$ , which is denoted by

a light shaded area, the value at Q' changes from 1 to 0. The output of NOR gate G<sub>1</sub> is affected by the change at Q'. After the propagation delay in G<sub>1</sub>, as denoted by a darker shaded area in the timing diagram, Q becomes 0. The change of Q to 0 does not further affect the value of Q'. The circuit is now stable. From the above analysis, it is seen that, regardless of the present value of Q, Q is equal to 1 after S becomes 1 and R is 0.

At t<sub>1</sub>, the value of S returns to 0. The change does not affect the values of Q and Q'. At t<sub>2</sub>, R changes from 0 to 1, forcing the output of Q to change from 1 to 0. The transition at Q does not occur until t<sub>2</sub>' due to the propagation delay in G<sub>1</sub>. The change at Q again creates a change at Q' from 0 to 1, which does not happen until t<sub>2</sub>'' because of the delay in G<sub>2</sub>. Thus the next state is 0 if the present state is 1 and the present inputs are S = 0 and R = 1. The changes at t<sub>3</sub> and t<sub>4</sub> will not be elaborated and can be easily traced. However, note that at t<sub>5</sub>, both S and R are equal to 1, which force both Q and Q' to be 0. This violates the assumption that the two latch outputs are complementary to each other. Thus the present input combination of SR = 11 is prohibited.

The characteristic table in Table 9.1 lists the next state Q<sup>+</sup> based on the present inputs S, R and the present state Q. When S = R = 0, the next state is the same of the present state. When S = 0, R = 1, despite what is the present state, the next state is 0. A next state of 1 is expected if S = 1 and R = 0. S = R = 1 is prohibited.

Table 9.1 Characteristic table for SR latch.

Present inputs S R		Present state Q	Next state Q <sup>+</sup>	Function	
0	0	0	0	Hold (No change)	t <sub>3</sub>
0	0	1	1		t <sub>1</sub>
0	1	0	0	Reset	t <sub>4</sub>
0	1	1	0		t <sub>2</sub>
1	0	0	1	Set	t <sub>0</sub> '
1	0	1	1		t <sub>0</sub>
1	1	0	d	Prohibited	t <sub>5</sub>
1	1	1	d		

The characteristic table can be converted to the form of a K-map as shown in Figure 9.5, which is called a next-state map. A Boolean expression known as characteristic equation can be obtained from the map.

Characteristic equation:  $Q^+ = S + R'Q$

The characteristic equation is valid only when the condition SR = 0 is satisfied. This condition precludes S = R = 1 to be the present inputs. Figure 9.6 is the logic symbol for SR latch.

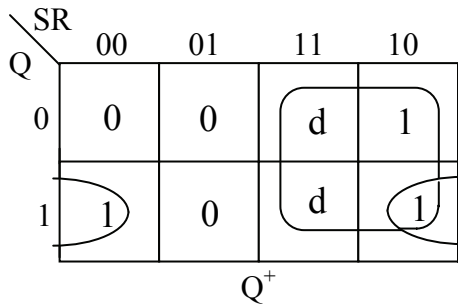


Figure 9.5 Next-state map for SR latch.

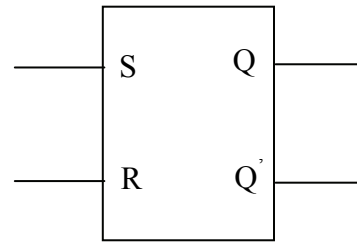


Figure 9.6 Logic symbol for SR latch.

### Gated SR Latch

The S and R inputs to the latch shown in Figure 9.7(a) are not applied directly to the SR latch made up of the cross-coupled NOR gates. Each of them is gated by an AND gate. The AND gates are controlled by a signal C. When C is equal to 0, both AND gates are closed and their outputs are 0. Thus Q is not affected by the S and R inputs applied to the AND gates. The latch can be considered as disabled in this case. When C is equal to 1, the gates are open, allowing S and R to propagate to the gate outputs, which become inputs to the latch. With the addition of two AND gates to control the passing or blocking of S and R to the inputs of the cross-coupled NOR circuit, the latch is called a gated latch. The logic symbol for gated SR latch is given in Figure 9.7(b).

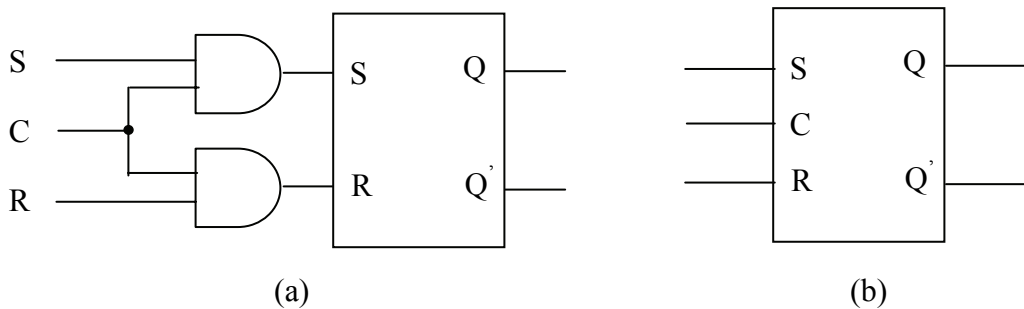


Figure 9.7 Gated SR latch. (a) Circuit structure. (b) Logic symbol.

## 9.3 Flip-Flops

### 9.3.1 Gated Latch as Flip-flop

As flip-flops are memory elements controlled by a clock, can the gated SR latch be used as a flip-flop by applying a clock to the control signal C? To examine this possibility, the behavior of a synchronous sequential circuit is further discussed. As time goes on, a clock proceeds from one clock cycle to the next clock cycle. A synchronous sequential circuit will advance from the present state toward the next state. The state

transition from the present state to the next state is signified by the change of one set of values in one clock cycle to another set of values in the following clock cycle at the flip-flop outputs. The two sets of values will be the same if the next state is the same as the present state. The state cannot change more than once in each clock cycle.

In Figure 9.1, assume that  $pdc$  is the propagation delay in the combinational portion of a sequential circuit and  $pdm$  the propagation delay in the memory. As shown in the timing diagram in Figure 9.8, the memory in Figure 9.1 is enabled when the clock is high. External inputs are applied to the sequential circuit at  $t_0$ . The excitations to the memory are ready at  $t_1$  after  $pdc$  seconds, waiting for the clock to go high. The state transition begins at  $t_2$  when the clock is high and is completed at  $t_3$  after  $pdm$  seconds. The next state, which is expected before the clock transition at  $t_2$ , now becomes the present state. The new state will travel through the combinational circuit, causing the excitations to change at  $t_4$ . Unfortunately the clock is still high at  $t_4$ . The enabling of the memory allows the excitations to propagate through the memory for another state transition. This violates the behavior of a synchronous sequential circuit. Thus a gated latch cannot be employed as a flip-flop.

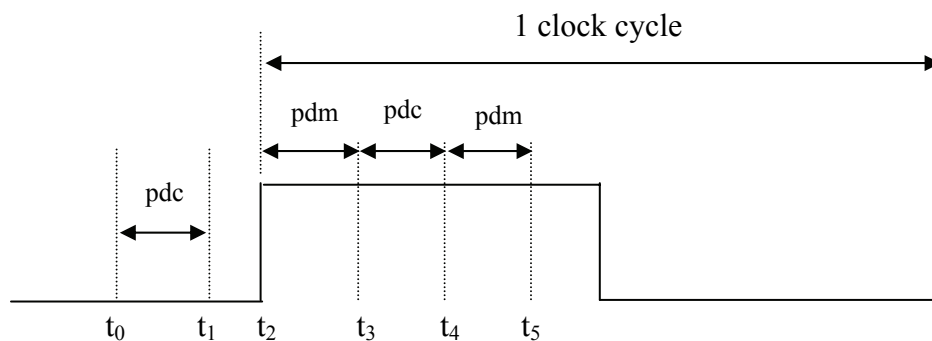


Figure 9.8 Timing diagram for a gated SR latch as a flip-flop.

### 9.3.2 Flip-Flops

#### Master-Slave SR Flip-Flop

As discussed in Section 9.3.1, a gated SR latch cannot function as a flip-flop because the states may undergo more than one transition in one clock cycle. The master-slave SR flip-flop in Figure 9.9 will eliminate such a problem. It consists of two gated SR latches in series. One of the latches is controlled by a clock pulse and the other latch by the complement of this clock pulse. Therefore when one latch is enabled or activated, the other is disabled or deactivated. The inputs  $S$  and  $R$  (outside the dashed box) to the flip-flop are connected to the  $S$  and  $R$  inputs of the master latch. The outputs of the master latch will then drive the  $S$  and  $R$  inputs of the slave. In other words, the master forces the  $Q$  and  $Q'$  outputs of the slave to have the same values as those of the master. The outputs from the slave are the outputs of the master-slave flip-flop.

When a set of inputs is applied to the flip-flop, the outputs of the master latch will respond to the inputs when the clock turns high and advance to a new state. The slave will not respond to this new state while the clock is still high, prohibiting any change at the outputs of the slave. Because the outputs of the flip-flop (or the state) do not change, the inputs to the combinational portion of the sequential circuit also remain intact. This again leaves the inputs to the master as well as the new state at the master outputs intact. When the clock goes low, the slave is activated, which allows the new state at the master outputs to drive the slave. The slave outputs will then assume the new state. The new state will then go through the combinational circuit to the inputs of the flip-flop, which are also the inputs to the master latch. Although the inputs to the master latch have changed, they will not affect the outputs of the master latch because the clock is still low and the slave is still enabled. When the master starts to respond to the input change, the clock must have turned high and it is a new clock cycle. Thus it is seen that with the master-slave structure, there will not be more than one state transition in each clock cycle.

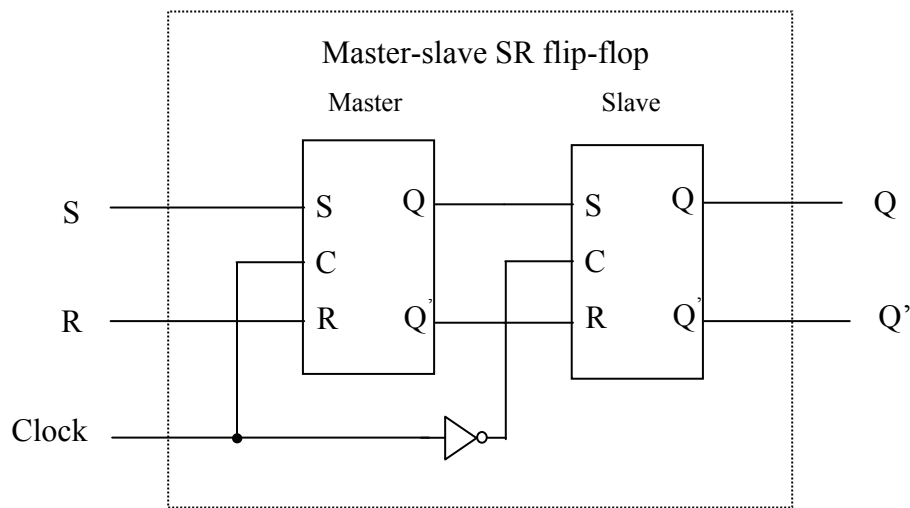


Figure 9.9 Master-slave SR flip-flop.

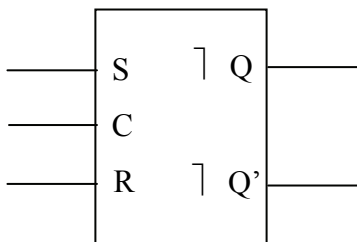


Figure 9.10 Logic symbol for SR flip-flop.

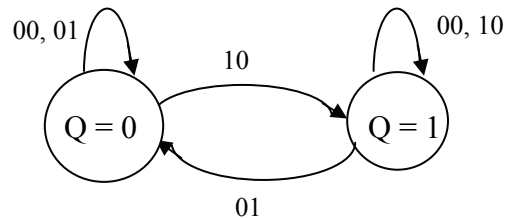


Figure 9.11 State diagram for SR flip-flop.

The master-slave flip-flop is a pulse-triggered flip-flop. The logic symbol is given in Figure 9.10. The symbol  $\nabla$  indicates that the flip-flop outputs will undergo changes at the transition of the clock from 1 to 0. If the master latch is triggered when the clock is

low and the slave is triggered when the clock is high. The symbol  $\downarrow$  will be used. Figure 9.11 is a graphical description of state transitions for a synchronous sequential circuit, which is called a state diagram. In a state diagram, each state is denoted by a circle. The state name or value is written inside the circle. The transition from one state to another is shown by a directed line. The value appended to a directed line specifies the present input values that lead to such a transition.

### JK Flip-Flop

JK flip-flops are an improvement to SR flip-flop. The J and K inputs to a JK flip-flop are analogous to the S and R inputs to a SR flip-flop. J and K are used to set and reset respectively. However, both J and K are allowed to be 1. When  $J = K = 1$ , the flip-flop output is toggled. The next state is the complement of the present state. The structure of the JK flip-flop is given in Figure 9.12(a) using a SR flip-flop. The logic symbol is given in Figure 9.12(b).

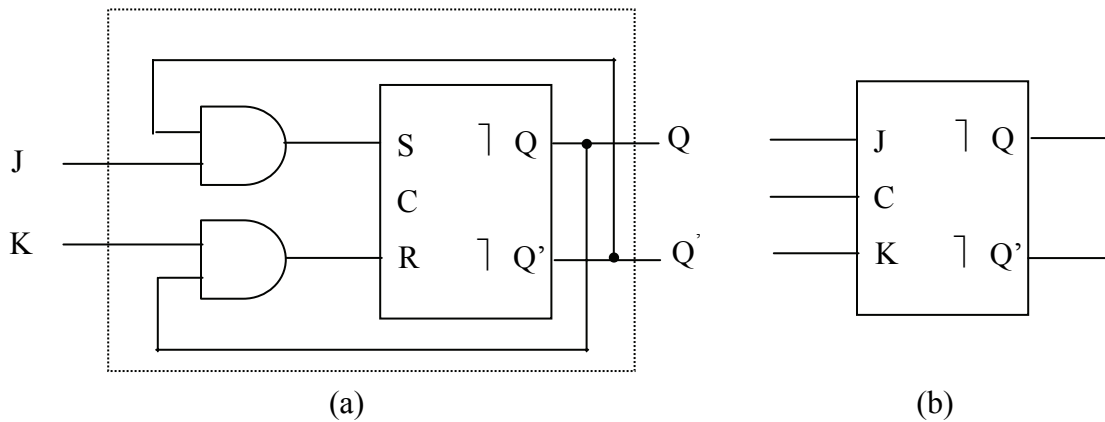


Figure 9.12 JK flip-flop. (a) Circuit structure. (b) Logic symbol.

Table 9.2 Characteristic table for JK flip-flop.

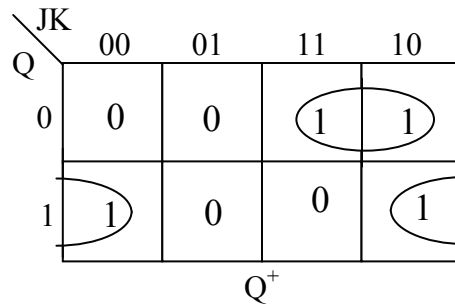
Present inputs J K		Present state Q	S = $JQ'$	R = $KQ$	Next state $Q^+$	Function
0	0	0	0	0	0	Hold (No change)
0	0	1	0	0	1	
0	1	0	0	0	0	Reset
0	1	1	0	1	0	
1	0	0	1	0	1	Set
1	0	1	0	0	1	
1	1	0	1	0	1	Toggle
1	1	1	0	1	0	



The characteristics of JK flip-flop is derived in Table 9.2 based on the circuit structure in Figure 9.12(a). The values of S and R listed in the third column of the table are derived from the values of J, K, and Q. The values of S, R, and Q are then used to determine  $Q^+$ . The characteristics are expressed in Figure 9.13 as a next-state map, from which the characteristic equation is obtained.

Characteristic equation:  $Q^+ = JQ' + K'Q$

Figure 9.13 Next-state map for JK flip-flop.



### D Flip-Flop

When the inputs to a JK flip-flop are related by  $J = K'$  as shown in Figure 9.14(a), the flip-flop can be characterized by just one input D and is called a D flip-flop. When  $D = 1$ ,  $J = 1$  and  $K = 0$ , then  $Q = 1$ . When  $D = 0$ ,  $J = 0$  and  $K = 1$ , then  $Q = 0$ . Thus it is apparent that Q follows D. A present input to D in a clock cycle is expected to appear at the flip-flop output Q in the following clock cycle. Data input is transferred to the output but delayed by one clock cycle. The characteristic table is derived and shown in Table 9.3. The characteristic equation is simply

$$Q^+ = D$$

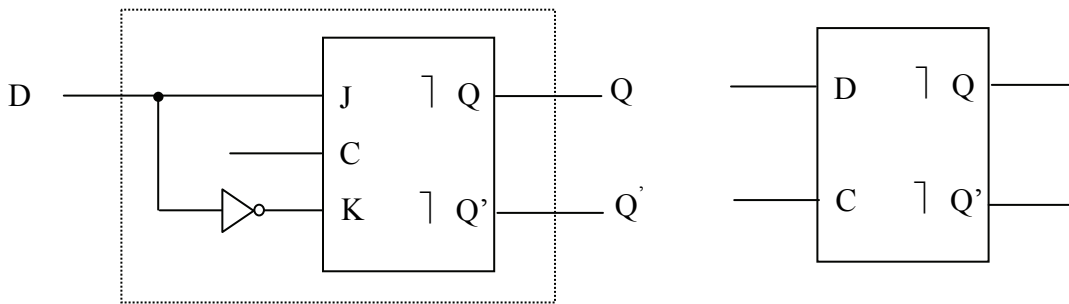


Figure 9.14 D flip-flop. (a) Circuit structure. (b) Logic symbol.

Table 9.3 Characteristic table for D flip-flop.

Present input D	Present state Q	J = D	K = D'	Next state Q <sup>+</sup>
0	0	0	1	0
0	1	0	1	0
1	0	1	0	1
1	1	1	0	1

### T Flip-Flop

As shown in Figure 9.15(a), when both inputs to a JK flip-flop are connected together, the flip-flop output will be either unchanged or toggled in the following clock cycle. This flip-flop is known as T flip-flop. When T = J = K = 0, the next state is the same as the present state. When T = J = K = 1, the next state is the complement of the present state. The logic symbol for T flip-flop is shown in Figure 9.15(b). The characteristics are listed in Table 9.4. The characteristic equation is

$$Q^+ = T \oplus Q$$

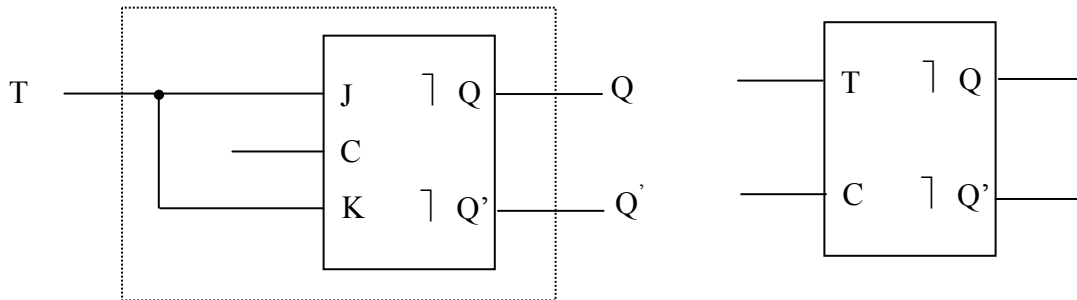


Figure 9.15 T flip-flop. (a) Circuit structure. (b) Logic symbol.

Table 9.4 Characteristic table for T flip-flop.

Present input T	Present state Q	J = T	K = T	Next state Q <sup>+</sup>
0	0	0	0	0
0	1	0	0	1
1	0	1	1	1
1	1	1	1	0

### 9.3.3 Edge-Triggered Flip-flops

All of the flip-flops introduced thus far are triggered by pulses. Inputs to a pulse-triggered flip-flop must remain constant while the master latch is activated. Edge-triggered flip-flops are operationally different from pulse-triggered flip-flops. Known as positive-edge-triggered and negative-edge-triggered, they are controlled respectively by the rising and falling edge of a clock pulse.

A timing diagram is shown in Figure 9.16 to explain the proper operation of a positive-edge-triggered D flip-flop. Before the positive edge of a clock pulse, the D input is applied to the flip-flop. The minimal time that allows the input to propagate to the output is called setup time  $t_{su}$ . The D input is also held constant for a certain duration called hold time  $t_h$  after the positive edge of the pulse. The hold time allows the clock input to propagate to the output of the flip-flop. Even though the clock is still high, any change at the D input will not affect the output of the flip-flop after the hold time. The constraints of setup time and hold time also apply to negative-edge triggered flip-flops. The logic symbols for edge-triggered flip-flops are given in Figure 9.17. A triangle is used instead of the symbols  $\lceil$  and  $\rfloor$ . This symbol is called a dynamic input indicator. The clock is connected to the dynamic input indicator. A bubble is placed before this symbol for negative edge-triggered flip-flops, as shown in Figure 9.17(b). Edge-triggered JK and T flip-flops have the same operational properties of edged-triggered D flip-flops.

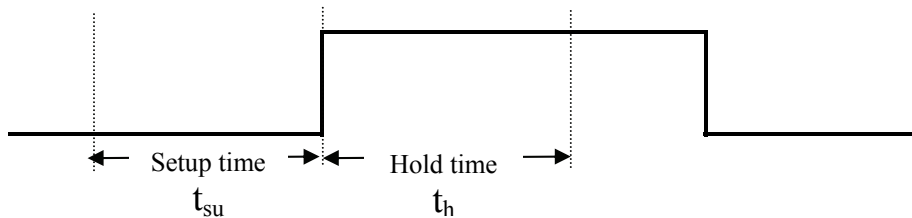


Figure 9.16 Timing constraint of positive-edge triggered flip-flop.

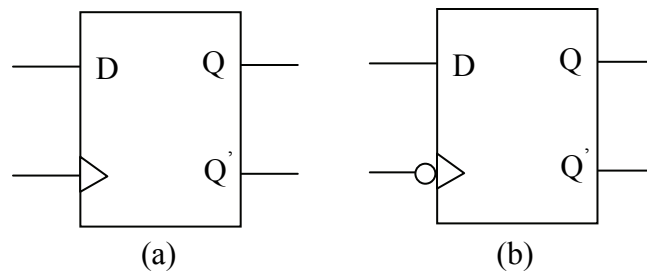


Figure 9.17 Logic symbols for edge-triggered flip-flop. (a) positive-edge. (b) Negative-edge.

### 9.3.4 Asynchronous Preset and Clear

Asynchronous preset and clear are additional features of flip-flops. When asserted, an asynchronous preset will force the flip-flop to a 1-state. The assertion of asynchronous clear on the other hand will force the flip-flop to a 0-state. Asynchronous preset and clear are not triggered by a clock. They override the flip-flop input(s) and the clock. They are used to initialize a sequential circuit so that operations can start from a certain condition or state. The logic symbols for a positive edge-triggered flip-flop and a negative-edge triggered flip-flop with active-low asynchronous preset and clear are shown in Figure 9.18. If the active-low signal names are placed outside the rectangle and before the bubbles, a slash is added to the front of the names. The slash is omitted if the names are displayed inside the rectangle.

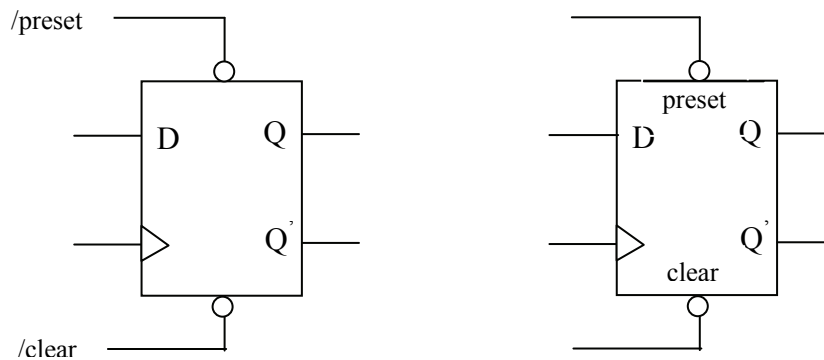


Figure 9.18 Logic symbols for flip-flops with asynchronous preset and clear.

The timing diagrams in Figure 9.19 illustrate the change of Q for a positive edge-triggered D flip-flop with active low asynchronous preset and clear. Propagation delays are not taken into account. How Q attains its value is explained and listed below.

- |                    |   |
|--------------------|---|
| $t_0 \leq t < t_1$ | /clear is asserted. $Q = 0$ .   |
| $t_1 \leq t < t_2$ | Both /clear and /preset are not asserted. No positive edge of clock. Flip-flop is idle. The value of Q does not change. |
| $t_2 \leq t < t_3$ | Both /clear and /preset are not asserted. Flip-flop is triggered at $t_2$ . $Q = 1$ .                                   |
| $t_3 \leq t < t_4$ | /preset is asserted. $Q = 1$ .  |
| $t_4 \leq t < t_5$ | Both /clear and /preset are not asserted. No positive edge of clock. Flip-flop is idle. The value of Q does not change. |
| $t_5 \leq t < t_6$ | Both /clear and /preset are not asserted. Flip-flop is triggered at $t_6$ . $Q = 1$ .                                   |
| $t_7 \leq t$       | Both /clear and /preset are not asserted. Flip-flop is triggered at $t_7$ .   |

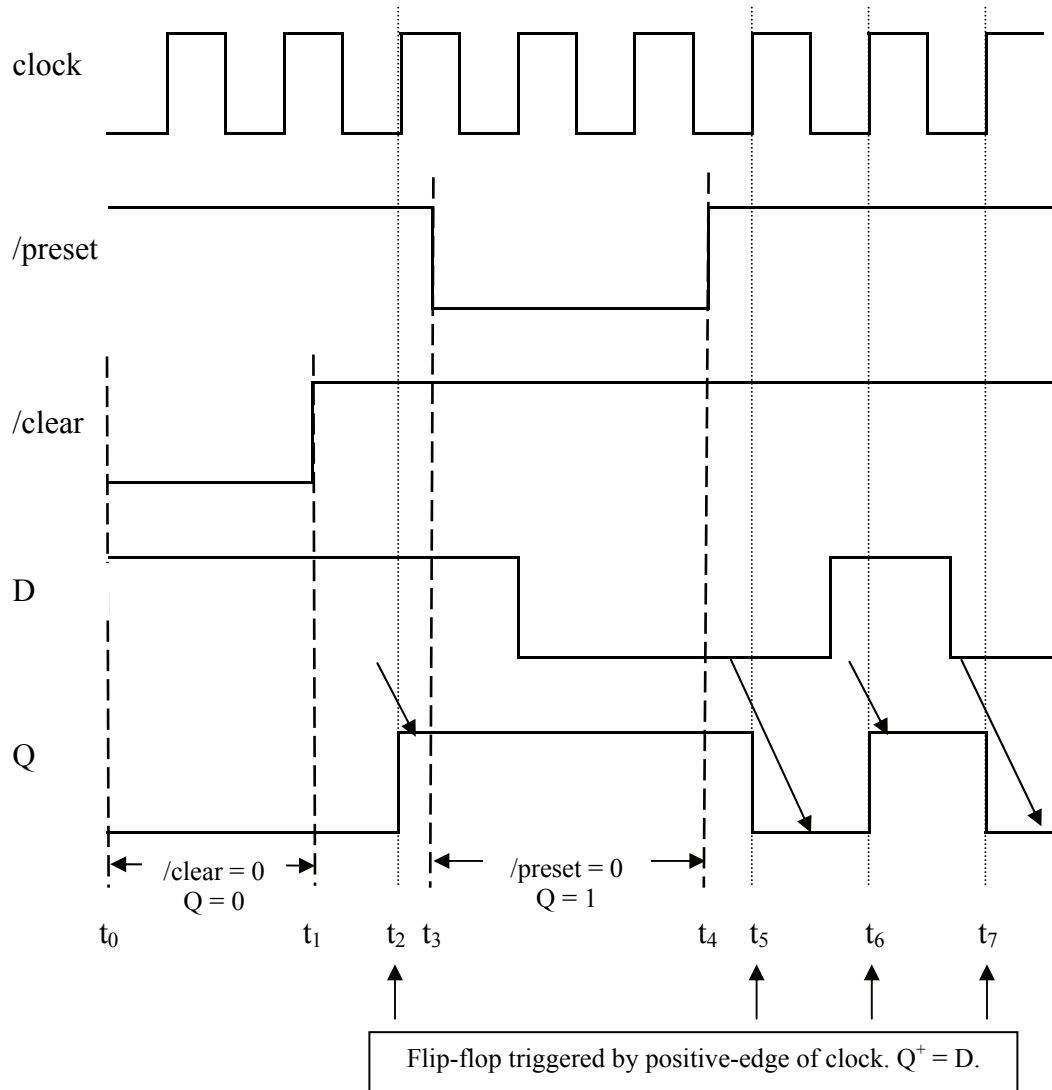


Figure 9.19 Timing diagrams for a positive edge-triggered D flip-flop with asynchronous preset and clear.

## PROBLEMS

1. Draw the state diagram for (a) D flip-flops, (b) T flip-flops, and (c) JK flip-flops.
2. Draw the state diagram and find the characteristic equation for a MN flip-flop with the following characteristics.

When  $MN = 00$ , the next state  $Q^+$  is equal to 1 (set).  
 When  $MN = 01$ , the next state  $Q^+$  is the same as the present state  $Q$  (no change).  
 When  $MN = 10$ , the next state  $Q^+$  is the complement of the present state  $Q$  (toggled).  
 When  $MN = 11$ , the next state  $Q^+$  is equal to 0 (reset).

3. For the xy latch in Figure P9.1, (a) find the characteristic table, (b) find the characteristic equation, and (c) draw the state diagram.
4. Given in Figure P.9.2 are the timing diagrams for the input to a positive-edge-triggered D flip-flop and for the active-low asynchronous preset and clear. Draw the timing diagram for the flip-flop output  $Q$ .
5. Given in Figure P.9.3 are the timing diagrams for the inputs to a positive-edge-triggered JK flip-flop and for the active-low asynchronous preset and clear. Draw the timing diagram for the flip-flop output  $Q$ .

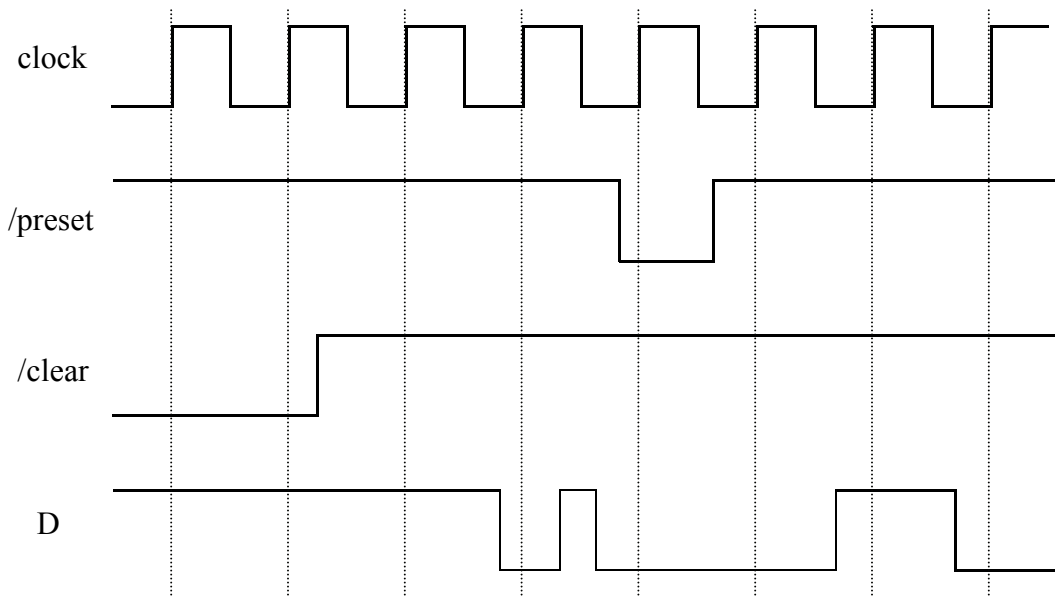
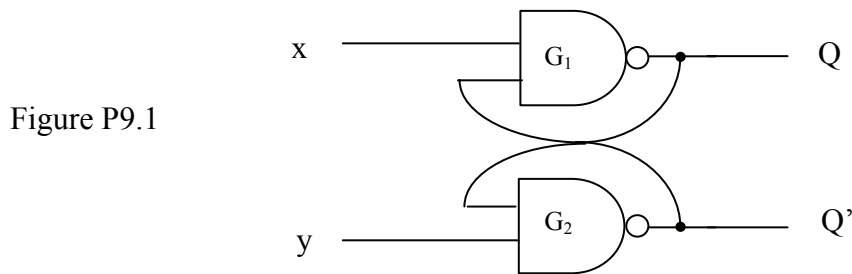


Figure P9.2

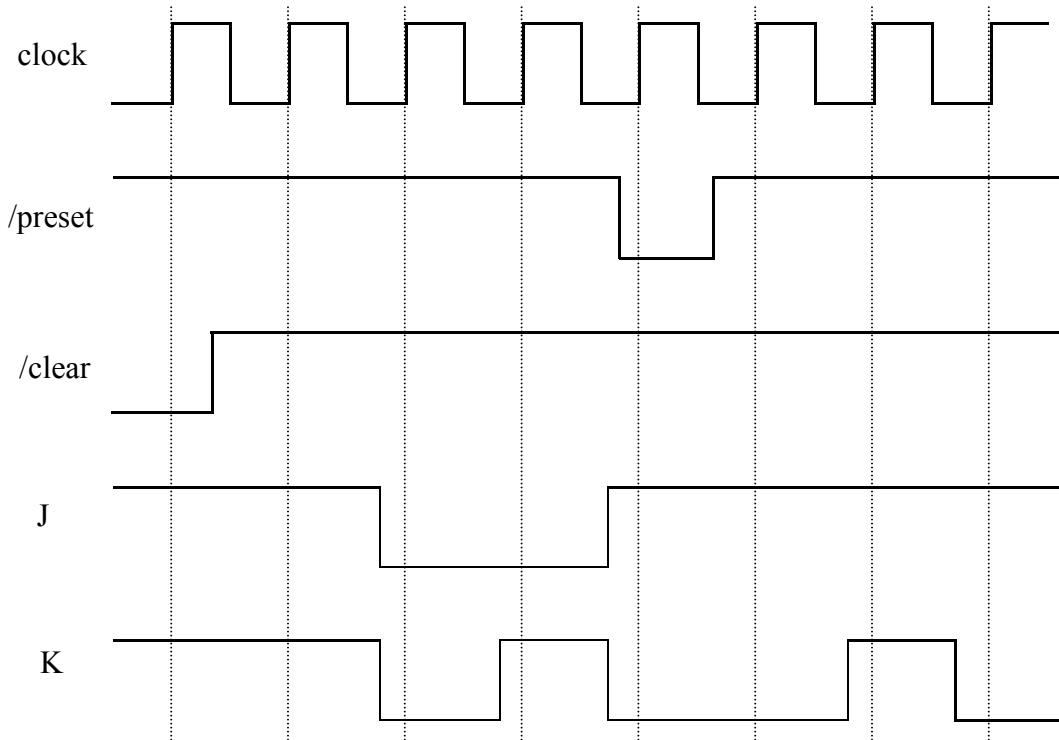


Figure P9.3

