CHAPTER 10

SYNCHRONOUS SEQUENTIAL CIRCUITS

Registers and counters, two very common synchronous sequential circuits, are introduced in this chapter. Register is a digital circuit for storing information. Contents of registers can also be manipulated for purposes other than storage. A counter is a device that performs state transitions. Analysis and synthesis of synchronous sequential circuits are also introduced in this chapter.

10.1 Registers

An n-bit register is a circuit that can store n bits of information. Every bit in a register is assigned a position number. The position numbers ranges from 0 to n-1, with 0 assigned to the rightmost bit and incremented toward the left. Since a flip-flop can store one bit of information, a register can be constructed from n flip-flops. Figure 10.1(a) shows the bit positions and the contents of a 4-bit register. The contents are $Q_2Q_2Q_1Q_0$. Figure 10.1(b) shows the circuit of a 4-bit register. When a 4-bit data $a_3a_2a_1a_0$ is applied to the inputs of the four D flip-flops, they will be stored in the register when the flips-flops are triggered by the positive edge of a clock pulse.

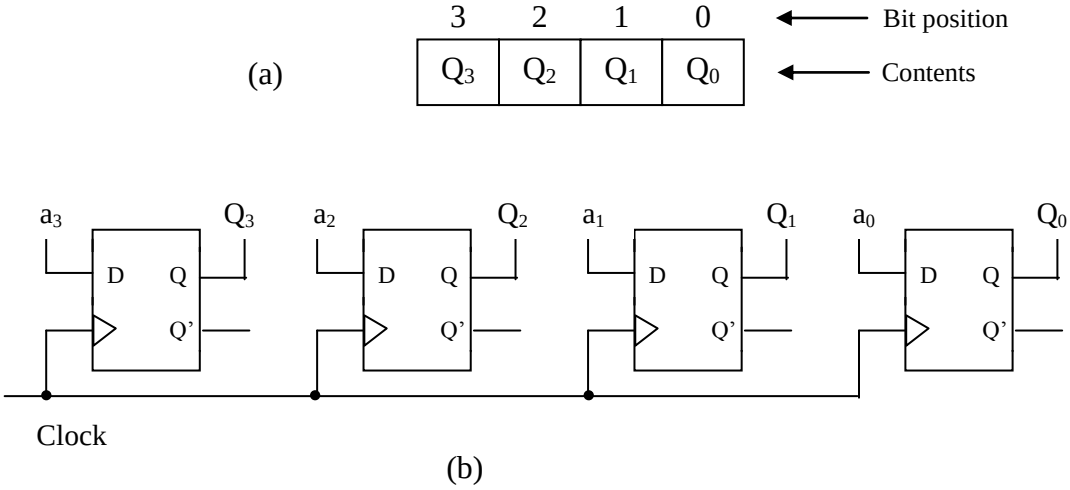
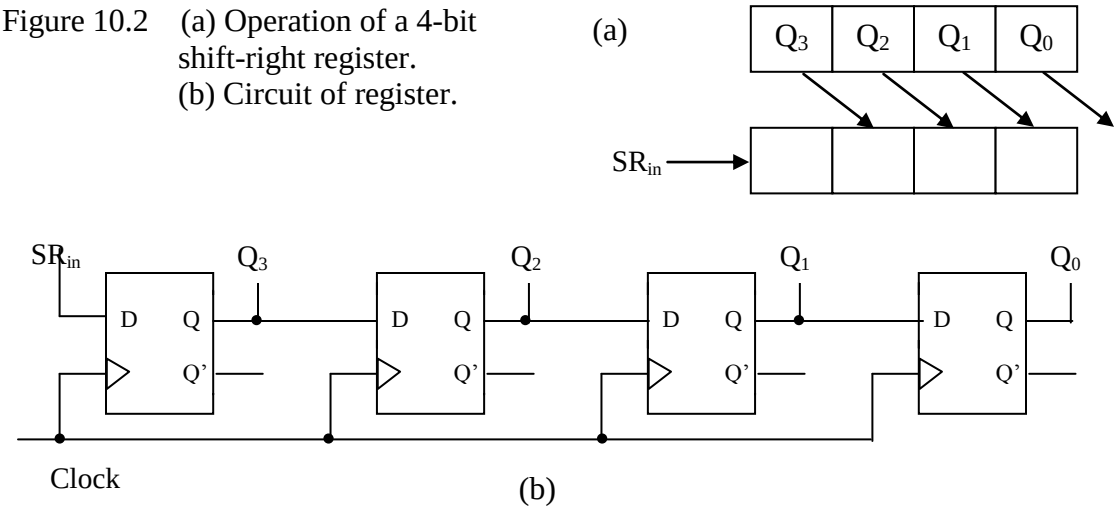


Figure 10.1 (a) Notation for a 4-bit register. (b) Circuit for a 4-bit register.

The usage of a register is limited if it can only store information. A shift register not only can store information but also can shift its contents to either right or left. The operation of a 4-bit shift-right register is shown in Figure 10.2(a). A circuit diagram for this register is given in Figure 10.2(b). $Q_3Q_2Q_1Q_0$ can be shifted to the right one bit in each clock cycle. SR_{in} is an external bit shifted into position 3. Q_0 is lost after the shift.

The contents are $SR_{in}\ Q_3Q_2Q_1$ after shifting. If Q_0 is connected to the D input of the leftmost flip-flop, i.e. $SR_{in} = Q_0$, the contents will be $Q_0Q_3Q_2Q_1$ after shifting. This is called a right rotation. Implementation of a shift-right register is simple. As shown in Figure 10.2(b), the output of one flip-flop is connected to the input of the next (less significant) flip-flop.

Figure 10.2 (a) Operation of a 4-bit shift-right register.
(b) Circuit of register.



A universal 4-bit shift-register that performs four different functions is introduced. The four functions are hold, shift right, shift left, and parallel load. The function "hold" leaves the contents of the register intact after the register is triggered by a clock pulse. Parallel load allows a 4-bit data to be loaded into the register following the positive edge of a clock pulse. The functions and the contents of the register after being triggered by a clock pulse are listed in Table 10.1. The function to be executed is defined by two selection signals s_1 and s_0.

Table 10.1 Function table for a 4-bit universal shift register.

Function	s_1 s_0	Contents			
		Bit position			
		3	2	1	0
Hold	0 0	Q_3	Q_2	Q_1	Q_0
Shift right	0 1	SR_{in}	Q_3	Q_2	Q_1
Shift left	1 0	Q_2	Q_1	Q_0	SL_{in}
Parallel load	1 1	a_3	a_2	a_1	a_0

Figure 10.3 is a design of the universal 4-bit shift register. A 4-to-1 multiplexer is used to select the data to be stored in each flip-flop. The right column in Table 10.1 lists

the contents of the register after an operation has been carried out. Therefore they are the inputs to the multiplexers as shown in Figure 10.3. SL_{in} is an external bit shifted into position 0 for left-shift. $a_3a_2a_1a_0$ is a 4-bit data to be loaded into the register.

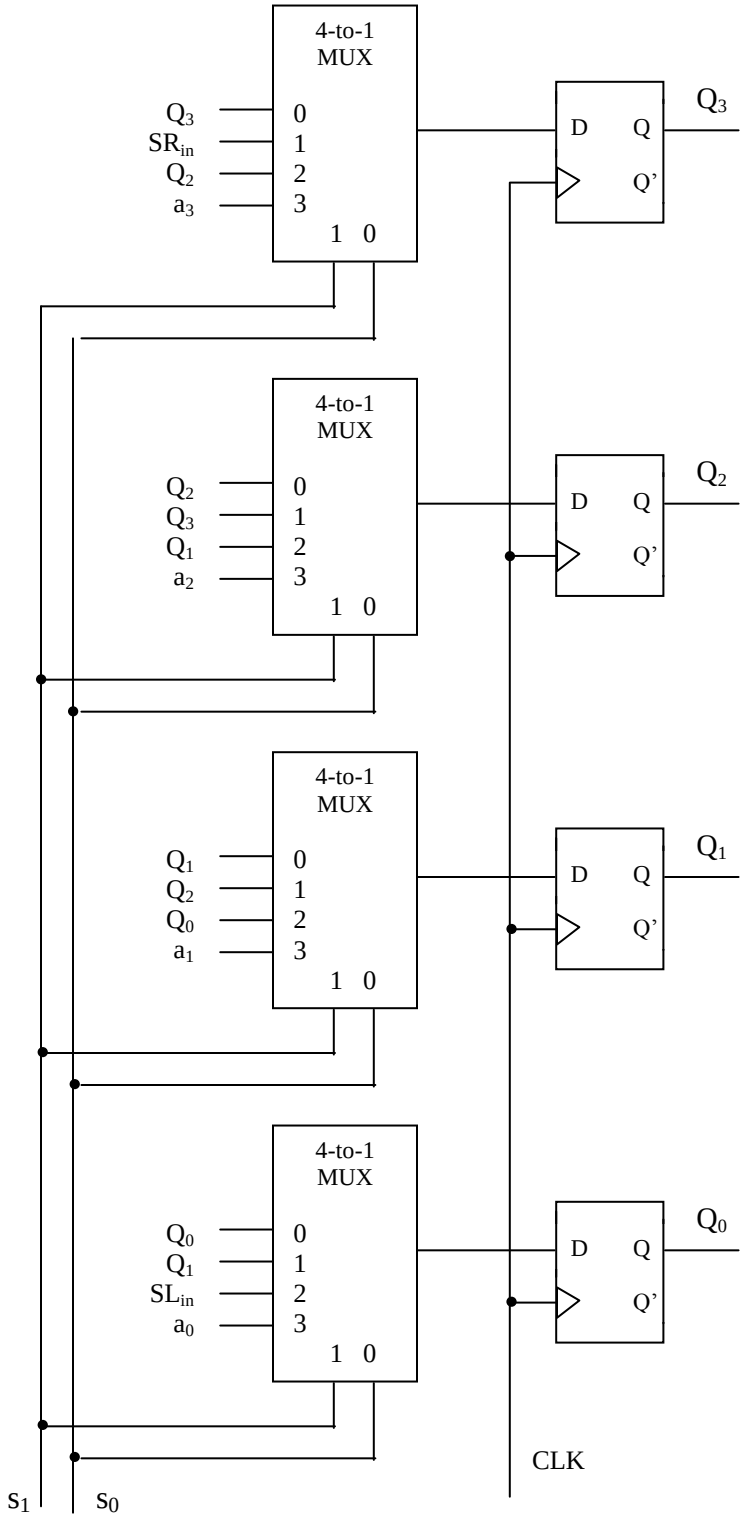


Figure 10.3 Design of a 4-bit universal shift register.

10.2 Counters

A counter is a synchronous sequential circuit that can generate a sequence of numbers or states. The sequence can be in descending, ascending, or random order. Figure10.4 is the state diagram of a counter of six different states. It is called a 6-state counter. The sequence is repeated every six clock cycles. Assume 000 is the initial state, followed by five other states in the order of 110, 001, 100, 101, and 011. The three binary values are the outputs Q_2, Q_1, and Q_0 of three flip-flops used to implement the counter. The timing diagrams for the counter are shown in Figure 10.5.

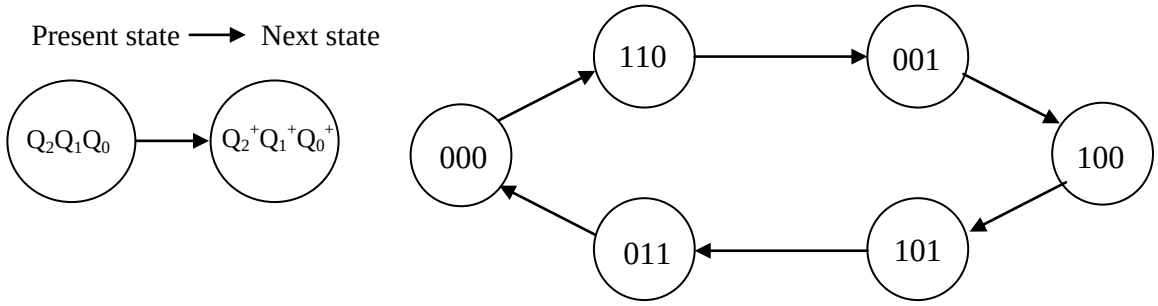


Figure 10.4 State diagram of a 6-state counter.

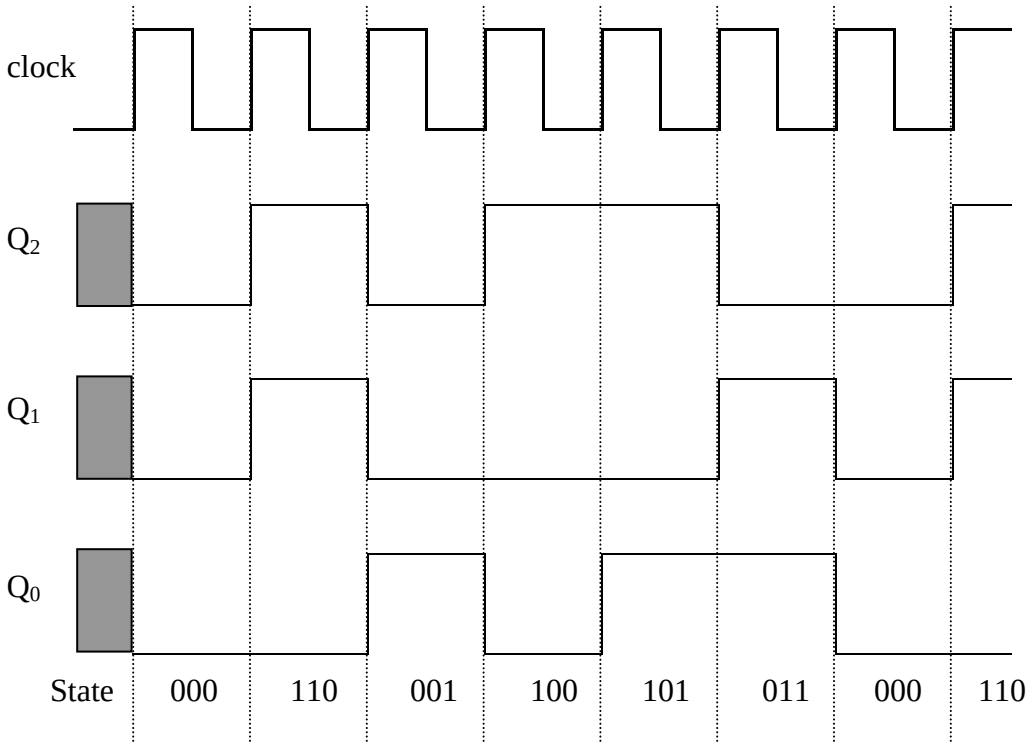


Figure 10.5 Timing diagram of the 6-state counter in Figure 10.4.

Ring Counter

In a ring counter, each state is represented by one flip-flop. An n-state ring counter requires n flip-flops. In each state, only one flip-flop output is asserted and all the others are de-asserted. In other words, only one flip-flop output is 1 and all the other flip-flop outputs are 0. Table 10.2 is the state assignment table for a 4-bit or 4-state ring counter. The four states are named T_0, T_1, T_2, and T_3. State assignment is to assign a combination of flip-flop output values to a state, or vice versa. The state diagram of the 4-bit ring counter is shown in Figure 10.6. The asserted output is shifted from left to right and

Table 10.2 State assignment table for a 4-state ring counter

State	Q_0 Q_1 Q_2 Q_3
T_0	1 0 0 0
T_1	0 1 0 0
T_2	0 0 1 0
T_3	0 0 0 1

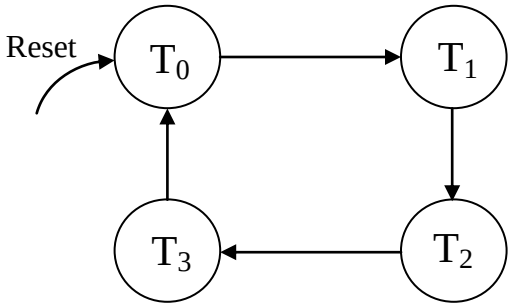


Figure 10.6 State diagram of a 4-state ring counter.

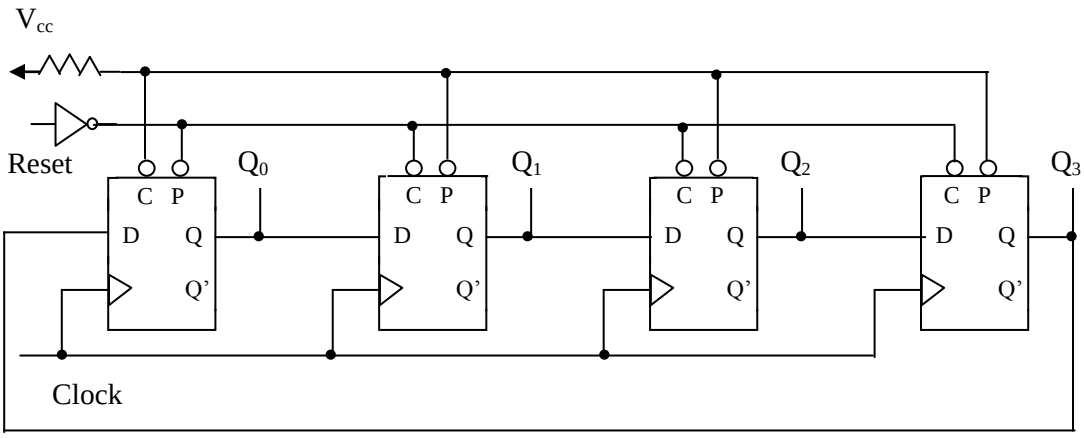


Figure 10.7 Circuit diagram for a 4-bit ring counter.

is rotated to the leftmost position from the rightmost position. The state transition is $T_0 \rightarrow T_1 \rightarrow T_2 \rightarrow T_3 \rightarrow T_0$ ……. Figure 10.7 is the circuit diagram for the 4-state ring counter. Note that it is essentially a right-rotate register. Asynchronous clear (C) and preset (P) are used to initialized the counter to the initial state T_0 by applying a positive pulse to the "Reset" input. All asynchronous preset and clear inputs are de-asserted during normal counting.

10.3 Analysis of Synchronous Sequential Circuits

Analysis is the reverse of synthesis or design. It is a process to understand the function of a circuit. Two models of synchronous sequential circuits are used to show the procedure in analysis.

Moore Model

The circuit diagram for a synchronous sequential circuit of Moore model is given in Figure 10.8. The circuit has one input x, one output Z, and two JK flip-flops. The combinational portion of the sequential circuit consists of one AND gate and one XOR gate. The analysis can be carried out in a number of steps.

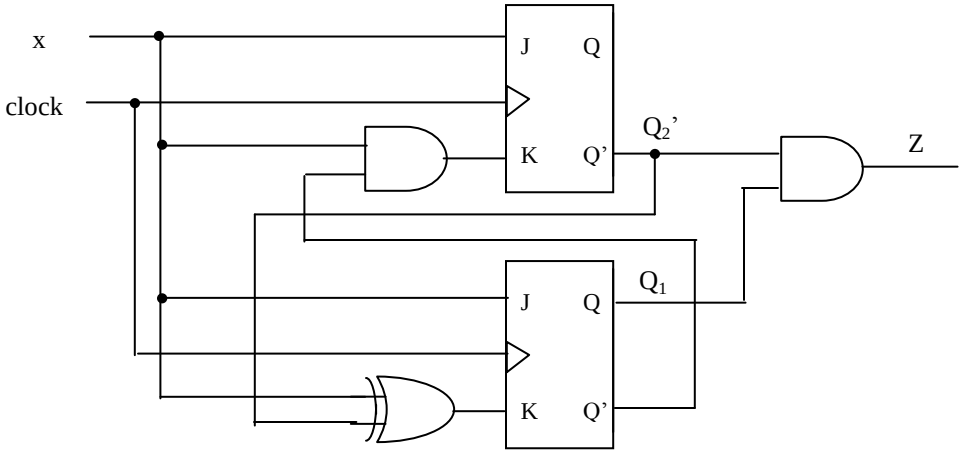


Figure 10.8 Synchronous sequential circuit of Moore model for analysis.

Step 1: Write the excitation and output functions.

$J_2 = x$ $\quad K_2 = x\,Q_1'$
$J_1 = x$ $\quad K_1 = x \oplus Q_2'$
$Z = Q_2'Q_1$

Step 2: Substitute the excitation functions into the characteristic equations for the two flip-flops to get the next-state equations.

$$Q_2^+ = J_2Q_2' + K_2'Q_2 = xQ_2' + (x\,Q_1')'Q_2 = \; xQ_2' + x'Q_2 + Q_2Q_1$$

$$Q_1^+ = J_1Q_1' + K_1'Q_1 = xQ_1' + (x \oplus Q_2')'Q_1 = xQ_1' + x'Q_2Q_1 + xQ_2'Q_1$$

Step 3: Convert the next-state equations to next-state maps.

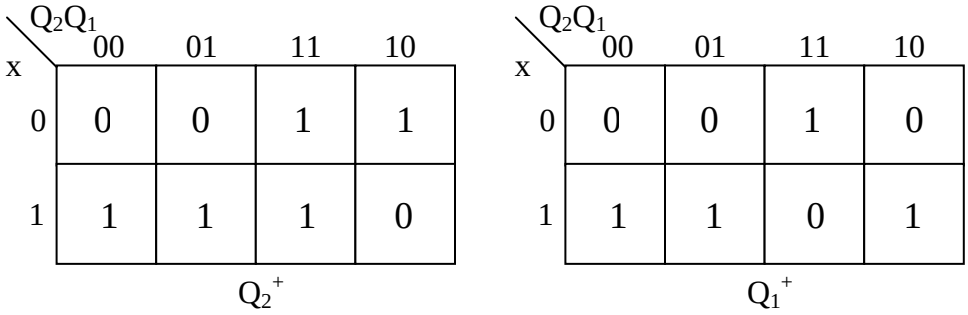


Figure 10.9 Next-state maps.

Step 4: Convert the next-state maps to a table. The table is called a transition table because it shows the transition from present states to next states. If the output is also included in the table, it is called a transition/output table.

Table 10.3 Transition/output table.

Q_2Q_1	$Q_2^+\ Q_1^+$		Z
	x = 0	x = 1	
0 0	0 0	1 1	0
0 1	0 0	1 1	1
1 1	1 1	1 0	0
1 0	1 0	0 1	0

Step 5: Replace the states in the transition/output table using the state assignment in Table 10.4. The transition/output table is converted to a state/output table.

Table 10.4 State assignment.

Q_2Q_1	State
0 0	A
0 1	B
1 1	C
1 0	D

Table 10.5 State/output table.

Present state	Next state		Z
	x = 0	x = 1	
A	A	C	0
B	A	C	1
C	C	D	0
D	D	B	0

Step 6: Convert the state/output table to a state diagram.

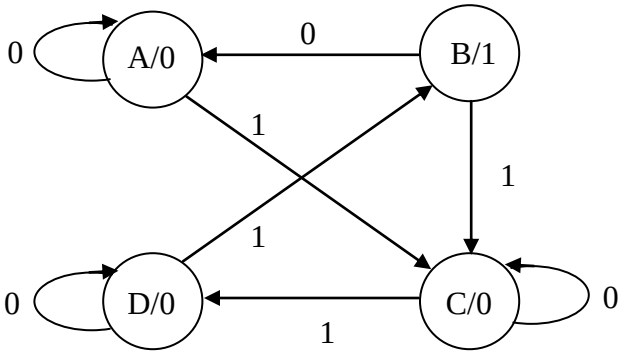


Figure 10.10 Moore model state diagram.

In this example, the output of the circuit is a function of Q_2 and Q_1. It does not depend on the present input of x. Therefore the output is placed together with the state name inside the circle. A synchronous sequential circuit is called a Moore model machine if the outputs are functions of the present state but not of the present inputs. A synchronous sequential circuit with a finite number of states is also called a finite-state machine.

Mealy Model

The circuit in Figure 10.11 is a sequential circuit of Mealy model. The output of this circuit depends on the present state as well as the present input x. The procedure for analyzing a Mealy model machine and a Moore model machine are the same, except some minor differences due to different types of outputs.

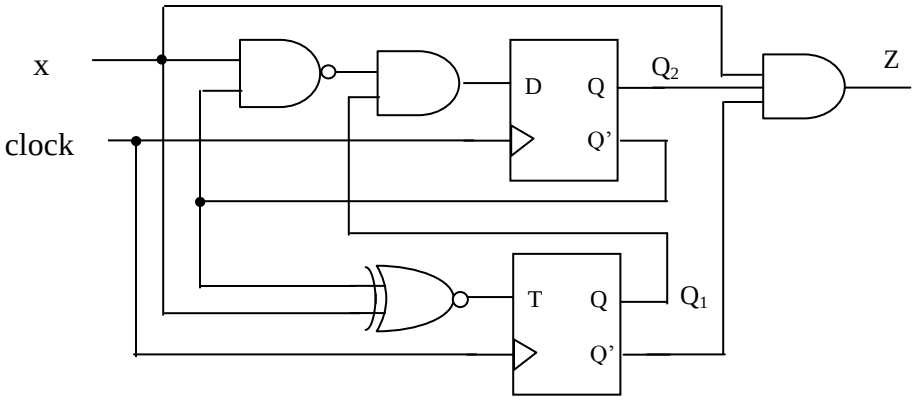


Figure 10.11 Synchronous sequential circuit of Mealy model for analysis.

Step 1: Write the excitation and output functions.

$$D_2 = (xQ_2')'Q_1$$

$$T_1 = x \odot Q_2' = (x \oplus Q_2')' = x \oplus Q_2$$

$$Z = xQ_2Q_1'$$

Step 2: Substitute the excitation functions into the characteristic equations to get the next-state equations.

$$Q_2^+ = D_2 = (xQ_2')'Q_1 = x'Q_1 + Q_2Q_1$$

$$Q_1^+ = T_1 \oplus Q_1 = x \oplus Q_2 \oplus Q_1$$

Step 3: Convert the next-state equations to next-state maps. Q_1^+ is the same as the function in Example 5.6.

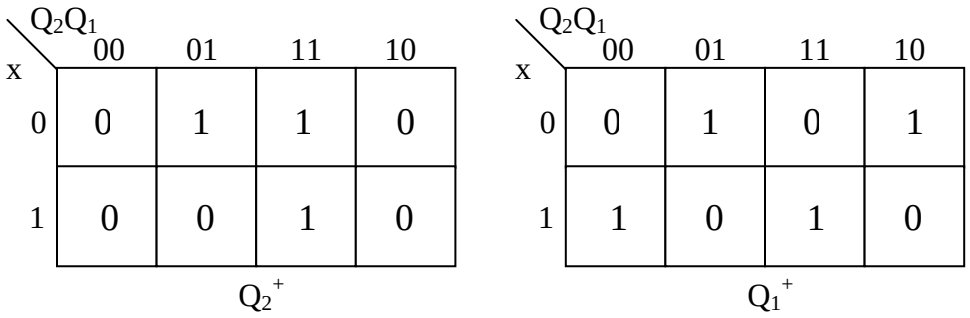


Figure 10.12 Next-state maps.

Step 4: Convert the next-state maps to a transition/output table. Note that the values of Z do not have to be listed separately. They are placed next to the values of $Q_2^+Q_1^+$ because Z is also a function of Q_2, Q_1, and x.

Table 10.6 Transition/output table.

Q_2Q_1	$Q_2^+ Q_1^+$, Z	
	x = 0	x = 1
0 0	0 0, 0	0 1, 0
0 1	1 1, 0	0 0, 0
1 1	1 0, 0	1 1, 0
1 0	0 1, 0	0 0, 1

Step 5: Convert the transition/output table to a state/output table using the state assignment in Table 10.7.

Table 10.7 State assignment.

Q_2Q_1	State
0 0	A
0 1	B
1 1	C
1 0	D

Table 10.8 State/output table.

Present state	Next state, output	
	x = 0	x = 1
A	A, 0	B, 0
B	C, 0	A, 0
C	D, 0	C, 0
D	B, 0	A, 1

Step 6: Convert the state/output table to a state diagram. Because Z is a function of the present state and the input x, its values are placed after x and separated by a slash.

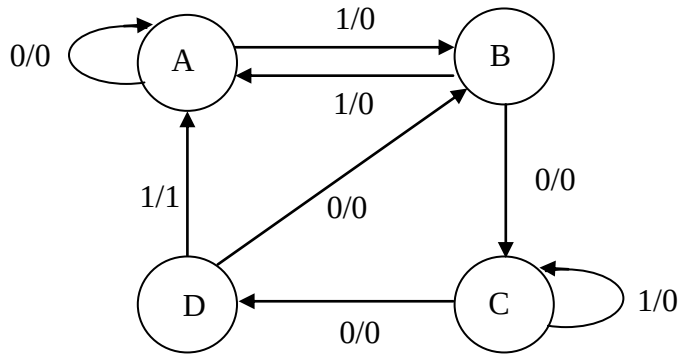


Figure 10.13 Mealy model state diagram.

10.4 Design of Counters

The design of a logic circuit usually starts with a word description of the function or behavior of the circuit. In synchronous sequential circuit design, a state diagram is usually constructed first from the word description. Construction of a state diagram probably is the most difficult step in the design procedure. Lack of understanding in the behavior of a circuit may lead to an incorrect state diagram. Sample inputs and their corresponding outputs may be drawn in the form of timing diagrams or in other forms to better understand the behavior of the circuit. The rest of the design procedure can more or less follow the analysis procedure in reverse order.

10.4.1 Counter Design

The design of an 8-state counter is given to illustrate the design procedure. The sequence is in the order of 0, 1, 2, 3, 4, 5, 6, 7, 0 ..... More specifically, it is called a modulo-8 counter. The state that is also the outputs is $Q_2Q_1Q_0$. As shown in Table 10.9, a transition table, after being constructed from the state diagram in Figure 10.14, is converted to three next-state maps in Figure 10.15. The next-state equations can be obtained directly from the next-state maps.

$$Q_2^+ = Q_2'Q_1Q_0 + Q_2Q_0' + Q_2Q_1' = Q_2'Q_1Q_0 + (Q_0' + Q_1')\,Q_2$$

$$= (Q_1Q_0)\,Q_2' + (Q_1Q_0)'\,Q_2 = (Q_1Q_0) \oplus Q_2$$

$$Q_1^+ = Q_1Q_0' + Q_1'Q_0 = Q_1 \oplus Q_0$$

$$Q_0^+ = Q_0'$$

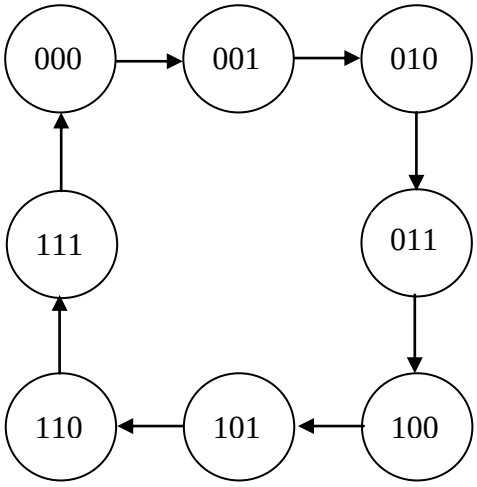


Figure 10.14 State diagram for a modulo-8 counter.

Table 10.9 Transition table for modulo-8 counter.

Present state $Q_2Q_1Q_0$	Next state $Q_2^+Q_1^+Q_0^+$
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	1 0 1
1 0 1	1 1 0
1 1 0	1 1 1
1 1 1	0 0 0

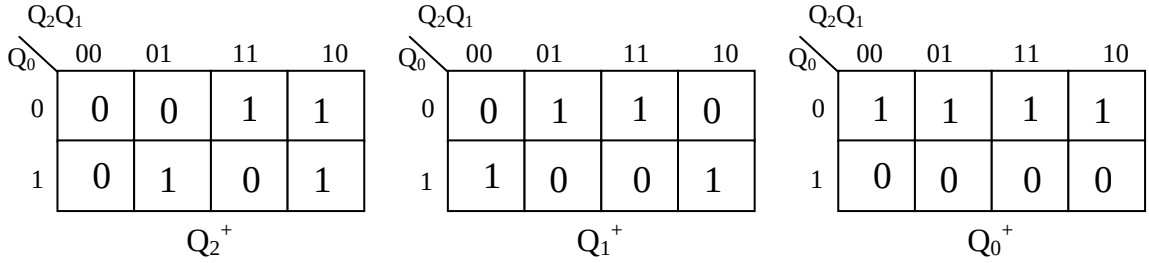


Figure 10.15 Next-state maps for modulo-8 counter.

The next step is to determine the excitation functions. It is necessary to decide what type of flip-flops to use in the design before the excitation functions can be determined. The use of D flip-flops will first be demonstrated because of its simple characteristic.

Design with D Flip-Flops

Because the excitation is the same as the next state for D flip-flops, the excitation functions are available without further derivations. Figure 10.16 is the circuit diagram of the counter using D flip-flops.

$D_2 = Q_2^+ = (Q_1Q_0) \oplus Q_2$
$D_1 = Q_1^+ = Q_1 \oplus Q_0$
$D_0 = Q_0^+ = Q_0'$

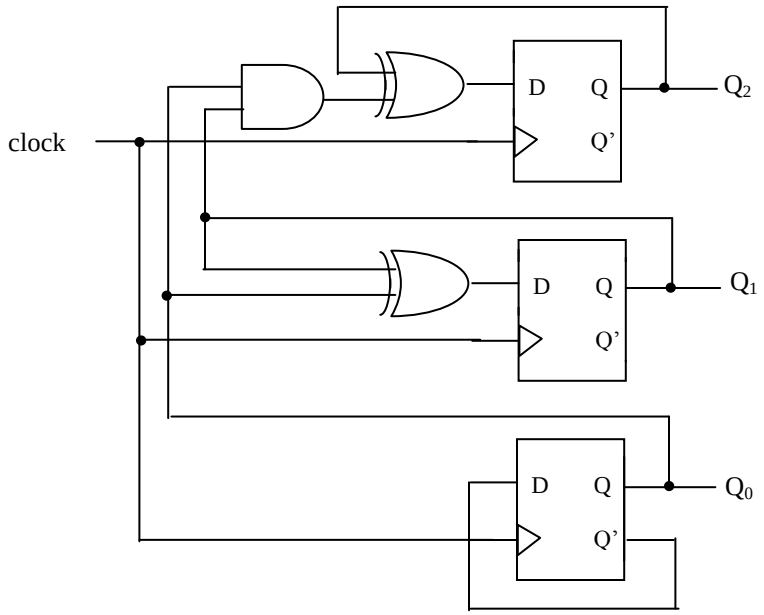


Figure 10.16 Circuit diagram for modulo-8 counter.

Design with JK Flip-Flops by Excitation Table

In analysis, the next-state equations are obtained by substituting the excitation functions into the characteristic equations. Q^+ is a function of the excitations or flip-flop inputs and the present state Q. In design, the excitations are to be determined from Q^+ and Q. The information of Q^+ and Q is given by the next-state maps or next-state equations. The characteristic table for JK flip-flops provides Q^+ if J, K, and Q are given. The excitation table determines the values of J and K if Q^+ and Q are given. The excitation table for JK flip-flops is given in Table 10.10. From the table, it is seen that each combination of Q and Q^+ values can result from two different functions of JK flip-flops. For example, for the transition of Q from 0 to 0, it can be either "no change" or "reset". The JK values for those two functions are 00 and 01 respectively. Thus the value of J is 0. The value of K can be either 0 or 1, which is denoted by a don't-care value "d".

By using the excitation table, the flip-flop inputs J_i and K_i for i = 0, 1, 2 can be determined as shown in Table 10.11. The first two columns are the transition table in

Table 10.9. To determine the excitations for state transitions, the transition from $Q_2Q_1Q_0$ = 001 to 010 is explained. For the transition of Q_2 from 0 to 0, $J_2 = 0$ and $K_2 = d$. For Q_1 to change from 0 to 1, $J_1 = 1$ and $K_1 = d$. For Q_0 to change from 0 to 1, $J_0 = d$ and $K_0 = 1$. After the excitations have been determined, Table 10.11 becomes the truth table for all J_i and K_i after removing the high-lighted column for $Q_2^+Q_1^+Q_0^+$.

Table 10.10 Excitation table for JK flip-flops.

Q	Q^+	J	K	Function
0	0	0	d	No change (JK = 00) or reset (JK = 01)
0	1	1	d	Set (JK = 10) or toggled (JK = 11)
1	0	d	1	Reset (JK = 01) or toggle (JK = 11)
1	1	d	0	No change (JK = 00) or set (JK = 10)

Table 10.11 J and K excitations for a modulo-8 counter.

Present state $Q_2Q_1Q_0$	Next state $Q_2^+Q_1^+Q_0^+$	Excitations		
		J_2 K_2	J_1 K_1	J_0 K_0
0 0 0	0 0 1	0 d	0 d	1 d
0 0 1	0 1 0	0 d	1 d	d 1
0 1 0	0 1 1	0 d	d 0	1 d
0 1 1	1 0 0	1 d	d 1	d 1
1 0 0	1 0 1	d 0	0 d	1 d
1 0 1	1 1 0	d 0	1 d	d 1
1 1 0	1 1 1	d 0	d 0	1 d
1 1 1	0 0 0	d 1	d 1	d 1

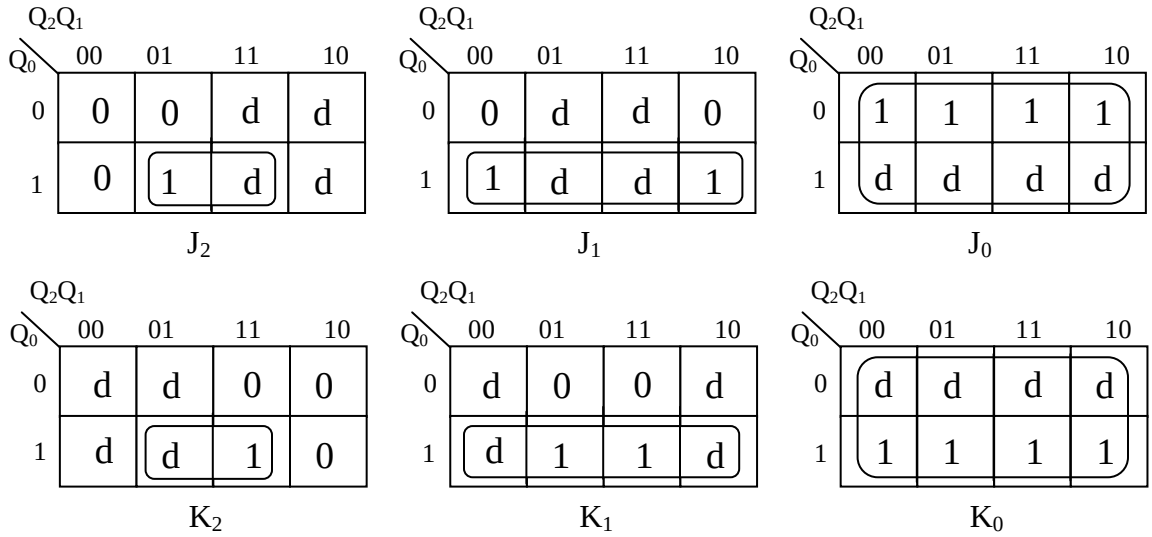


Figure 10.17 K-maps for excitation functions.

The K-maps for the excitation functions in Table 10.11 are plotted in Figure 10.17. The simplest sum-of-products expressions for the excitation functions are

$J_2 = Q_1Q_0$ $\quad$ $J_1 = Q_0$ $\quad$ $J_0 = 1$

$K_2 = Q_1Q_0$ $\quad$ $K_1 = Q_0$ $\quad$ $K_0 = 1$

Design with JK Flip-Flops by Partition

Design of synchronous sequential circuits with JK flip-flops using the excitation table is straightforward but tedious. A better method that partitions a next-state map into two sub-maps, one for J and one for K', is introduced. If a synchronous sequential circuit consists of n JK flip-flops and A set of external inputs X, the next-state equation Q_i^+ for flip-flop i is a function of all the flip-flop outputs and X. As shown below, Q_i^+ can be expanded to two sub-functions by Shannon's expansion theorem.

$$Q_i^+(Q_{n-1}, Q_{n-2}, ..., Q_i, ... , Q_1, Q_0, X)$$
$$= Q_i' \bullet Q_i^+(Q_{n-1}, Q_{n-2}, ..., Q_i = 0, ... , Q_1, Q_0, X)$$
$$+ Q_i \bullet Q_i^+(Q_{n-1}, Q_{n-2}, ..., Q_i = 1, ... , Q_1, Q_0, X)$$

By comparing the above equation with the characteristic equation of JK flip-flops which is

$$Q_i^+ = J_iQ_i' + K_i'Q_i$$

It is seen that J_i and K_i' are in fact the two sub-functions of Q_i^+ with Q_i as the expansion variable.

$$J_i = Q_i^+(Q_{n-1}, Q_{n-2}, ..., Q_i = 0, ... , Q_1, Q_0, x_{m-1}, x_{m-2}, ..., x_1, x_0) = (Q_i^+)_{Qi = 0}$$

$$K_i' = Q_i^+(Q_{n-1}, Q_{n-2}, ..., Q_i = 1, ... , Q_1, Q_0, x_{m-1}, x_{m-2}, ..., x_1, x_0) = (Q_i^+)_{Qi = 1}$$

The expansion of the next-state equation for Q_i is shown in the following binary diagram.

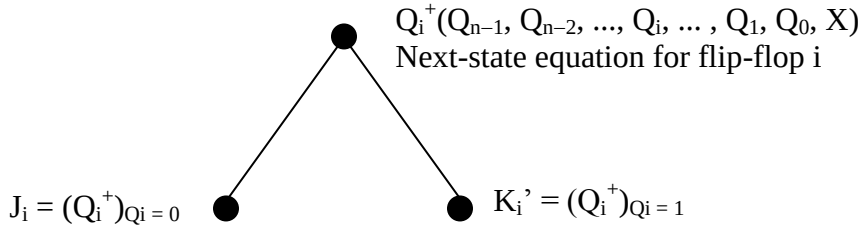


Figure 10.18 Expansion of next-state equation into J and K excitations.

From the next state equations of the modulo-8 counter, which are

$$Q_2^+ = (Q_1Q_0) \oplus Q_2$$

$$Q_1^+ = Q_1 \oplus Q_0$$

$$Q_0^+ = Q_0'$$

the excitation functions can be obtained as follows:

$$J_2 = (Q_2^+)_{Q2 = 0} = (Q_1Q_0) \oplus 0 = Q_1Q_0$$

$$K_2 = [(Q_2^+)_{Q2 = 1}]' = [(Q_1Q_0) \oplus 1]' = Q_1Q_0$$

$$J_1 = (Q_1^+)_{Q1 = 0} = 0 \oplus Q_0 = Q_0$$

$$K_1 = [(Q_1^+)_{Q1 = 1}]' = (1 \oplus Q_0)' = Q_0$$

$$J_0 = (Q_0^+)_{Q0 = 0} = 1$$

$$K_0 = [(Q_0^+)_{Q0 = 1}]' = 1$$

The results are identical to those using the excitation table.

Design with T Flip-Flops

A T flip-flop can perform two functions, either "no change" or "toggle". The excitation table can be readily constructed, as shown in Table 10.12. When $Q = Q^+$, it is "no change", T = 0. When $Q \neq Q^+$, the state is "toggle", T = 1. Therefore the excitation equation is

$$T = Q \oplus Q^+$$

Table 10.12 Excitation table for T flip-flops.

Q	Q^+	T	Function
0	0	0	Hold (No change)
0	1	1	Toggle
1	0	1	Toggle
1	1	0	Hold (No change)

The excitation functions for the modulo-8 counter can be obtained by substituting the next-state equations into the above equation.

$$T_2 = Q_2 \oplus Q_2^+ = Q_2 \oplus (Q_1\, Q_0) \oplus Q_2 = Q_1Q_0$$

$$T_1 = Q_1 \oplus Q_1^+ = Q_1 \oplus Q_1 \oplus Q_0 = Q_0$$

$$T_0 = Q_0 \oplus Q_0^+ = Q_0 \oplus Q_0' = 1$$

The K-maps for the excitation functions can also be derived directly from the next-state maps. By examining the excitation equation, it is apparent that $T_i = Q_i^+$ when $Q_i = 0$. When $Q_i = 1$, $T_i = (Q_i^+)'$. Therefore the K-map for T_i can be obtained from the next-state map Q_i^+ by complementing the portion in which $Q_i = 1$. The K-maps for T_2, T_1, and T_0 are shown in Figure 10.19. The highlighted portion in each map is the complement of the next-state map.

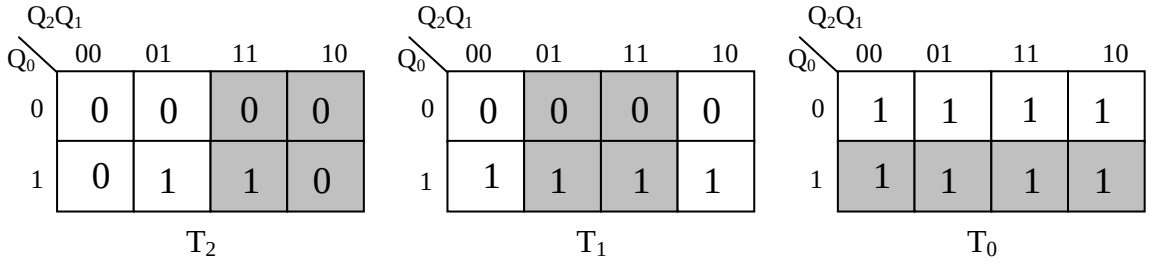


Figure 10.19 K-maps for the excitations of T flip-flops.

10.4.2 Self-Correcting Counter

The state diagram for a 6-state counter is given in Figure 10.20. The transitions of states are not in descending or ascending order. It is a random order. Three flip-flops are required in the implementation of this counter. States 2 and 7 are not used. They are called unused or invalid states. If for any reason the counter starts from an unused state or goes astray to one of the unused states, it should be able to return to the normal count sequence. Such a counter is said to be self-correcting.

Table 10.13 is the transition table. The next-state of an unused state is a don't-care state. Next-state verification for the two unused states is required at the completion of design to ensure that the counter is self-correcting. The following excitation functions are obtained from the next-state maps in Figure 10.21 if D flip-flops are used.

$$D_2 = Q_2^+ = Q_2'Q_1' + Q_1'Q_0'$$

$$D_1 = Q_1^+ = Q_2'Q_0' + Q_2Q_0 = (Q_2 \oplus Q_0)'$$

$$D_0 = Q_0^+ = Q_2$$

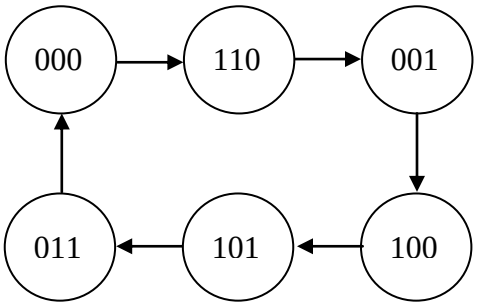


Figure 10.20 State diagram for a 6-state self-correcting counter.

Table 10.13 Transition table for a 6-state self-correcting counter.

Present state $Q_2Q_1Q_0$	Next state $Q_2^+Q_1^+Q_0^+$
0 0 0	1 1 0
0 0 1	1 0 0
0 1 0	d d d
0 1 1	0 0 0
1 0 0	1 0 1
1 0 1	0 1 1
1 1 0	0 0 1
1 1 1	d d d

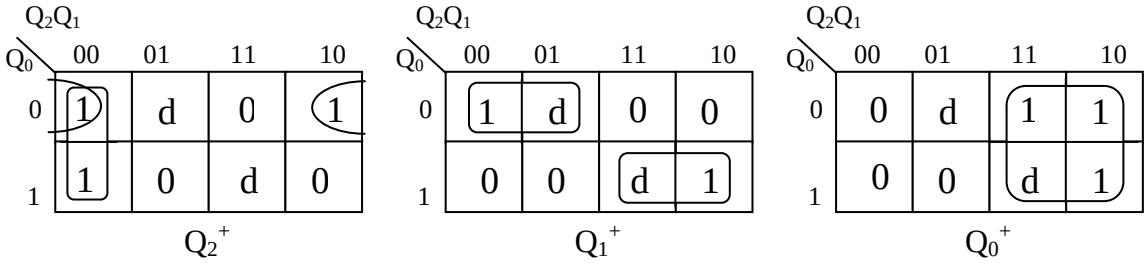


Figure 10.21 Next-state maps for the 6-state self-correcting counter.

The next-state of an unused state can be determined by substituting the values of $Q_2Q_1Q_0$ into the above equations. An easier approach is to examine the groupings of 1-cells on the next-state maps. A don't-care value is equal to 1 if it is grouped with 1-cells. Otherwise it is 0. Examination of the don't-care values on the next-state maps shows that the next states of 010 and 111 are 010 and 011 respectively. If the counter happens to be in the state 010, it will stay in this state forever and cannot return to the normal sequence. Since the counter is not self-correcting, a different design is necessary.

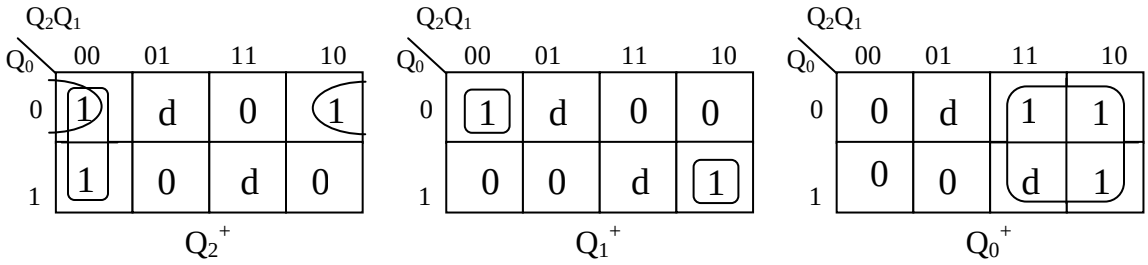


Figure 10.22 Re-design of the 6-state self-correcting counter.

In re-designing the counter, the don't-care terms on the next-state map Q_1^+ are left out in grouping. The groupings for Q_2^+ and Q_0^+ remain unchanged. The excitation function D_1 is

$$D_1 = Q_1^+ = Q_2'Q_1'Q_0' + Q_2Q_1'Q_0 = Q_1'(Q_2 \oplus Q_0)'$$

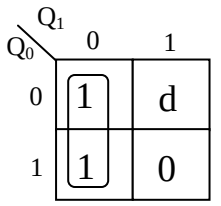
The next-states of 010 and 111 are now 000 and 001 respectively. Thus the counter is self-correcting.

To implement the counter using JK flip-flops, each of the next-state maps in Figure 10.21 is partitioned into two sub-function maps as shown in Figure 10.23. The K-maps in the second row of Figure 10.24 are the K-maps for K_2', K_1', and K_0'. They are inverted to the K-maps for K_2, K_1, and K_0 in the third row of the figure. The excitation functions are

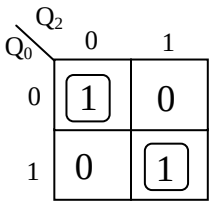
$J_2 = Q_1'$ $\qquad$ $K_2 = Q_1 + Q_0$

$J_1 = Q_2'Q_0' + Q_2Q_0 = (Q_2 \oplus Q_0)'$ $\qquad$ $K_1 = 1$

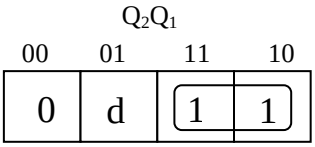
$J_0 = Q_2$ $\qquad$ $K_0 = Q_2'$



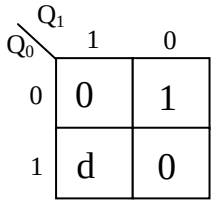
$J_2 = (Q_2^+)_{Q2 = 0}$



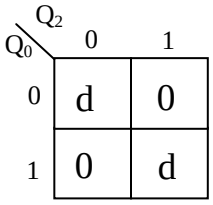
$J_1 = (Q_1^+)_{Q1 = 0}$



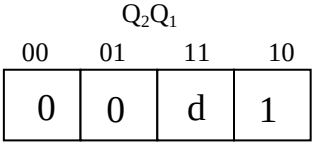
$J_0 = (Q_0^+)_{Q0 = 0}$



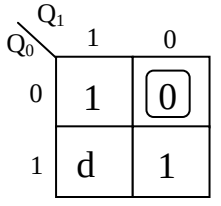
$K_2' = (Q_2^+)_{Q2 = 1}$



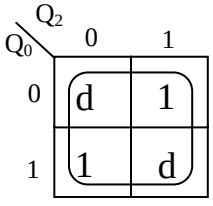
$K_1' = (Q_1^+)_{Q1 = 1}$



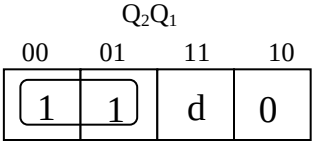
$K_0' = (Q_0^+)_{Q0 = 1}$



K_2



K_1



K_0

Figure 10.23 K-maps for JK excitations.

There are various ways to determine the next-states of the two unused states. One of them is to find the next state from the following next-state equations.

$$Q_2^+ = J_2Q_2' + K_2'Q_2 = Q_1'Q_2' + (Q_1 + Q_0)'Q_2 = Q_2'Q_1' + Q_2Q_1'Q_0'$$

$$Q_1^+ = J_1Q_1' + K_1'Q_1 = (Q_2 \oplus Q_0)'Q_1' + (1)'Q_1 = Q_2'Q1'Q_0' + Q_2Q_1'Q_0$$

$$Q_0^+ = J_0Q_0' + K_0'Q_0 = Q_2\,Q_0' + Q_2Q_0 = Q_2$$

By substituting $Q_2Q_1Q_0$ by 010 in the next-state equations, $Q_2^+Q_1^+Q_0^+ = 000$. With $Q_2Q_1Q_0 = 111$, the values of $Q_2^+Q_1^+Q_0^+$ in the next-state equations are 001.

Up-Down Self-Correcting Counter

The state diagram shown in Figure 10.24 is another example of a 6-state counter. However, the state transitions can also be in the reverse direction. It is called an up-down counter. Up-count and down-count are controlled by an external signal C. When C = 0, the counting is in the up or forward direction. When C = 1, the counting is in the down or backward direction. Next states are determined not only by present states but also by C. The transition table is given in Table 10.14. The next-state maps are shown in Figure 10.25. The counter is implemented using T flip-flops. The K-maps for T_2, T_1, and T_0 are obtained from the next-state maps in Figure 10.25 using the method developed in Section 10.4.1 and shown in Figure 10.26. The highlighted cells are the complements of the corresponding cells in Figure 10.26.

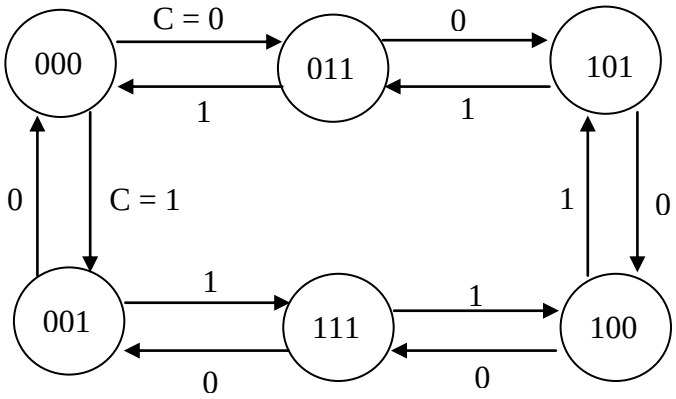


Figure 10.24 State diagram for a 6-state up-down counter.

The K-maps for the excitations in Figure 10.27 show high contents of XOR.

$$T_2 = C'Q_1Q_0 + CQ_1'\,Q_0 = Q_0\,(C \oplus Q_1)$$

$$T_1 = (C + Q_1 + Q_0')\,(C' + Q_1 + Q_0) = Q_1 + (C \oplus Q_0)'$$

$$T_0 = (C + Q_1' + Q_0')\,(C' + Q_1 + Q_0') = Q_0' + (C \oplus Q_1)'$$

Table 10.14 Transition table for a 6-state up-down counter.

Present state	Next state $Q_2^+Q_1^+Q_0^+$	
$Q_2Q_1Q_0$	C = 0	C = 1
0 0 0	0 1 1	0 0 1
0 0 1	0 0 0	1 1 1
0 1 0	d d d	d d d
0 1 1	1 0 1	0 0 0
1 0 0	1 1 1	1 0 1
1 0 1	1 0 0	0 1 1
1 1 0	d d d	d d d
1 1 1	0 0 1	1 0 0

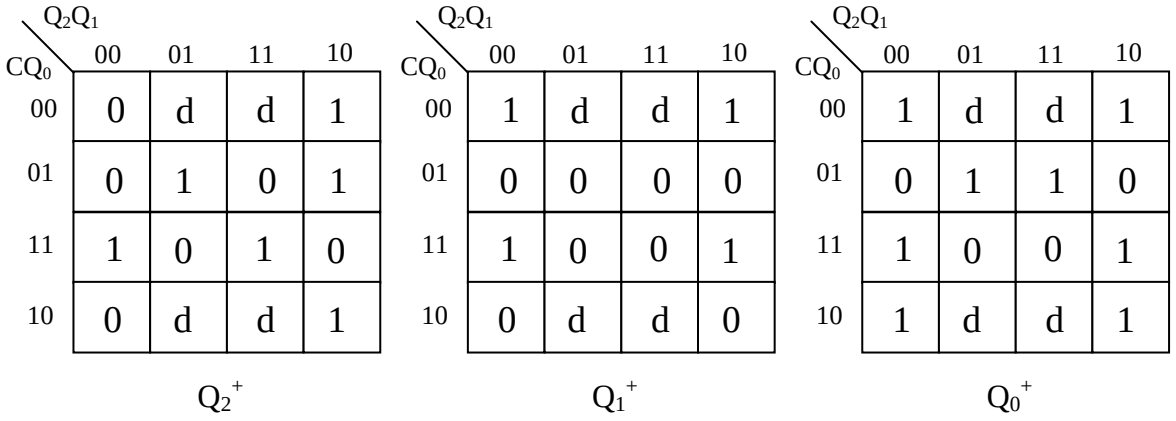


Figure 10.25 Next-state maps for a 6-state up-down counter.

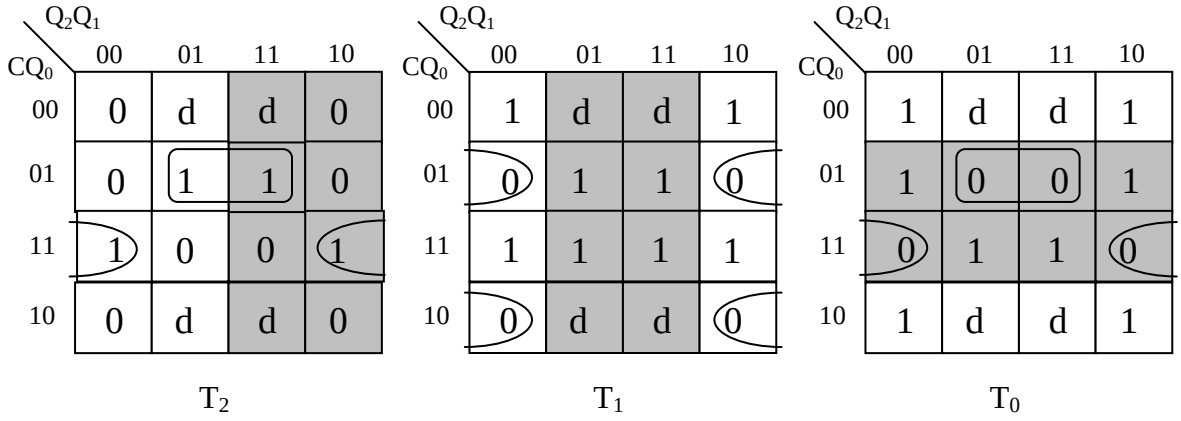


Figure 10.26 T excitations for the 6-state up-down counter in Figure 10.26.

The next states of the unused states can be read off directly from the K-maps for the excitations T_2, T_1, and T_0. Note that the values for the highlighted cells in Figure 10.26 should be complemented. The next-state maps obtained from Figure 10.26 are

shown in Figure 10.27. The next-states of the two unused state read from Figure 10.27 are as follows. They are independent of the value of C.

$Q_2Q_1Q_0 = 010$ $\quad Q_2^+Q_1^+Q_0^+ = 001$
$Q_2Q_1Q_0 = 110$ $\quad Q_2^+Q_1^+Q_0^+ = 101$

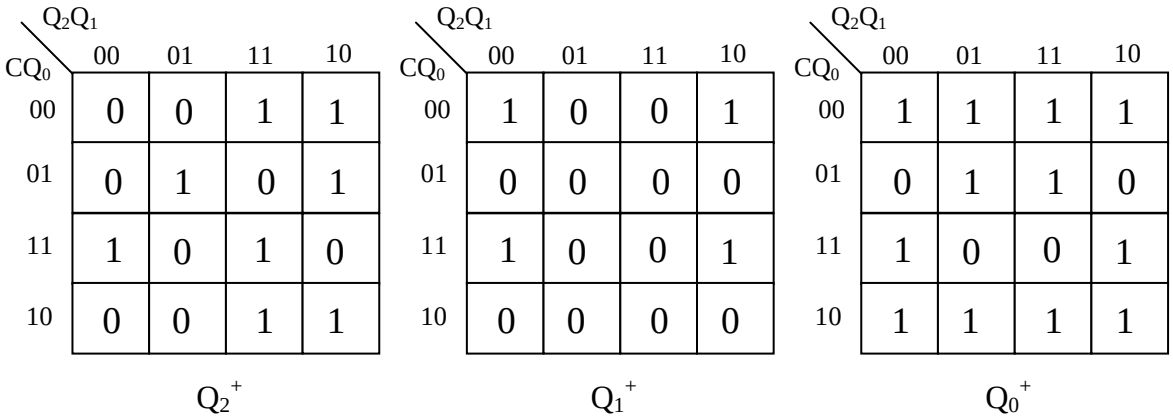


Figure 10.27 Next-state maps for a 6-state up-down counter after design.

10.5 Synthesis of Synchronous Sequential Circuits

In the design of a counter, the state diagram can be constructed very easily from a given counting sequence. In general, such is not the case for a synchronous sequential circuit. Sometimes, it is helpful to understand the problem by generating a sample input sequence and its corresponding output sequence. A bit-sequence detector or recognizer is used as an example. A bit-sequence detector is a synchronous sequential circuit to detect a specific sequence applied to a single input x. One bit is inputted to the circuit in each clock cycle. When a specific input sequence is detected, the output of the circuit becomes 1; otherwise the output is 0. The sequence to be detected in this example is a 3-bit sequence 101. After a sequence of 101 is detected, the circuit starts to detect the next sequence. No part in one sequence can be used as part of the next sequence. This is referred to as a non-overlapping sequence. The designs for both Moore model and Mealy model will be illustrated.

Moore Model

A sample sequence of input x and its corresponding output Z are listed in Table 10.15. All sequences of 101 are highlighted. The output will not become 1 until the clock cycle after the sequence has been detected. If Z becomes 1 in the same clock cycle as the third bit, the output is a function of the input. This is then a Mealy model. For instance, if Z = 1 in clock cycle 7 because of the input sequence in clock cycles 5, 6, and 7, what is

the value of Z in clock cycle 7 if the input x is 0 in clock cycle 7? Z will be 0, not 1. The value of Z in clock cycle 7 now depends on the value of x.

Table 10.15 Sample input/output sequence for a Moore model bit-sequence detector.

Clock cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Input x	1	1	0	0	1	0	1	0	1	0	1	1	0	1	….
Output Z	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1

Before constructing the state diagram, it is realized that four different conditions may occur during detection.

Condition A: Nothing has been detected, not even the first bit of the sequence.
Condition B: The first bit, 1, has been detected.
Condition C: The first two bits, 10, have been detected.
Condition D: All three bits, 101, have been detected.

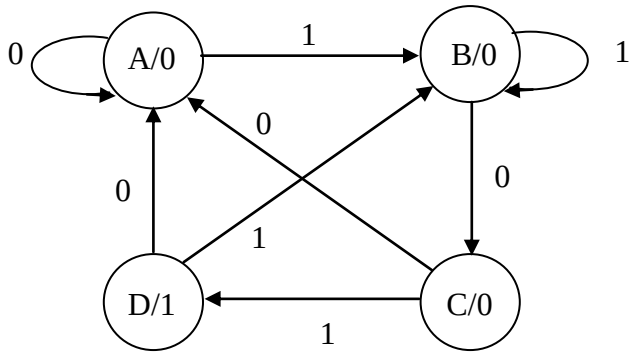


Figure 10.28 State diagram for a circuit of Moore model to detect 101.

Therefore, the minimum number of states is four. Sometimes, a state diagram with extra states may be constructed. The state diagram may still be correct. But this will increase the amount of components to be used. For example, four states can be represented by two flip-flops. Five states require three flip-flops. For one state diagram with six states and another with eight states, both need three flip-flops. However, the one with six states has two unused states, the next states of which are don't-care states. With more don't care terms on the next-state or excitation maps, the excitation functions may be simpler.

Various techniques can be used to minimize a state diagram. But it is not the topic in this chapter. Since the behavior of a synchronous sequential circuit can be described by a finite number of states. It is also called a finite-state machine.

The state diagram for the bit sequence detector is constructed in Figure 10.28 based on the four conditions. The state diagram is converted to a state/output table in Table 10.16. The next step is state assignment. For the four combinations of flip-flop output values, 00, 01, 10, and 11, one of them is assigned to state A. There are four choices. After one of them is selected for A, there are three combinations left for state B. Then there will be two combinations left for state C. Finally, only one combination is left for state D. Thus, there are $4\times3\times2\times1 = 24$ different ways to assign the four combinations of values to the four states. A good assignment will reduce the amount of components used to realize the circuit. The topic of how to get a good state assignment is not covered here. A random assignment as the one in Table 10.4 is used. The state/output table is transformed to a transition/output table in Table 10.17. The next-state maps are shown in Figure 10.29. They are partitioned to obtain the JK excitations in Figure 10.30. A circuit diagram is given in Figure 10.31.

$J_2 = x'Q_1$ $\quad\quad$ $K_2 = (xQ_1)'$

$J_1 = x$ $\quad\quad$ $K_1 = Q_2$

$Z = Q_2Q_1'$

Table 10.16 State/output table for bit-sequence detector.

Present state	Next state		Z
	x = 0	x = 1	
A	A	B	0
B	C	B	0
C	A	D	0
D	A	B	1

Table 10.17 Transition/output table for bit-sequence detector.

Q_2Q_1	$Q_2^+ Q_1^+$		Z
	x = 0	x = 1	
0 0	0 0	0 1	0
0 1	1 1	0 1	0
1 1	0 0	1 0	0
1 0	0 0	0 1	1

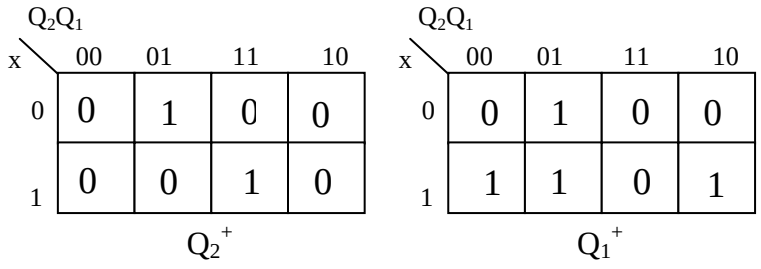


Figure 10.29 Next-state maps for the bit sequence detector.

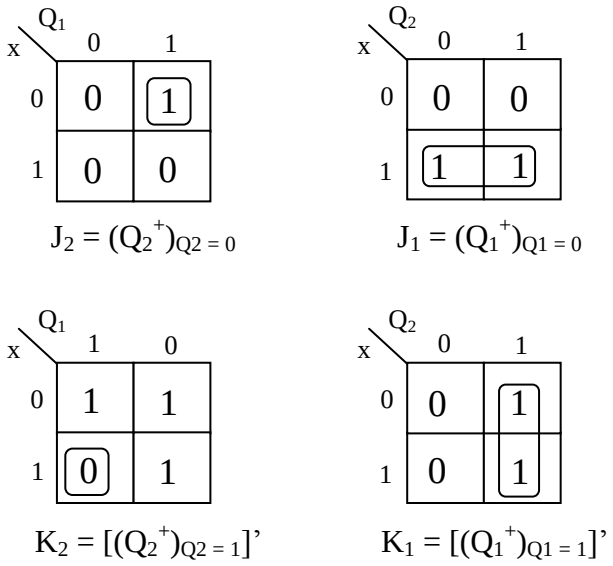


Figure 10.30 K-maps for the excitations of the bit sequence detector.

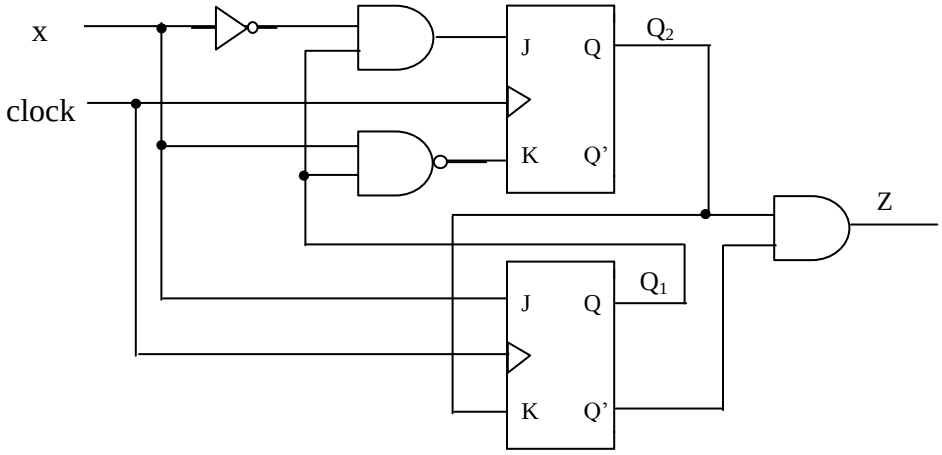


Figure 10.31 Sequential circuit of Moore model to detect a sequence of 101.

Mealy Model

To design the bit sequence detector for 101 as a Mealy model, a sample input/output sequence is given in Table 10.18. Overlapping is not allowed.

Table 10.18 Sample input/output sequence for a Mealy model bit-sequence detector.

Clock cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Input x	1	1	0	0	1	0	1	0	1	0	1	1	0	1	….
Output Z	0	0	0	0	0	0	1	0	0	0	1	0	0	1	….

For Mealy model, the output becomes 1 in the same clock cycle when the third bit of the sequence 101 is detected. There is no need to wait until the next clock cycle to generate an output of 1 and it saves one state. The three conditions required for a Mealy model are

Condition A: Nothing has been detected, not even the first bit of the sequence.
Condition B: The first bit, 1, has been detected.
Condition C: The first two bits, 10, have been detected. If present input x = 0, Z = 0. If x = 1, Z = 1.

The state diagram based on the above conditions is plotted in Figure 10.32. The state diagram is converted to a state/output table in Table 10.19. By using the following state assignments

$Q_2Q_1 = 00$ for states A
$Q_2Q_1 = 10$ for states B
$Q_2Q_1 = 11$ for states C
$Q_2Q_1 = 01$ Unused state

the state/output table is converted to the transition/output table in Table 10.20. Note that

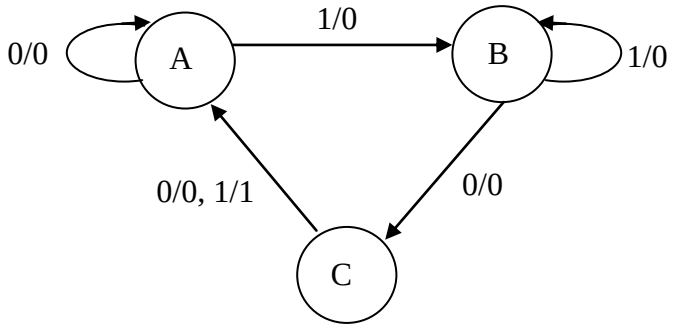


Figure 10.32 State diagram of a Mealy model circuit for detecting a sequence of 101.

Table 10.19 State/output table for bit-sequence detector.

Present state	Next state, Z	
	x = 0	x = 1
A	A, 0	B, 0
B	C, 0	B, 0
C	A, 0	A, 1

Table 10.20 Transition/output table for bit-sequence detector.

Q_2Q_1	$Q_2^+ Q_1^+$, Z	
	x = 0	x = 1
0 0	0 0, 0	1 0, 0
1 0	1 1, 0	1 0, 0
1 1	0 0, 0	0 0, 1
0 1	d d, d	d d, d

The transition/output table is further converted to two next state maps and the K-map for Z in Figure 10.33, from which the following excitation and output functions are obtained. A circuit diagram is given in Figure 10.34.

$J_2 = x$ $\quad K_2 = Q_1$

$J_1 = x'Q_2$ $\quad K_1 = 1$

$Z = xQ_1$

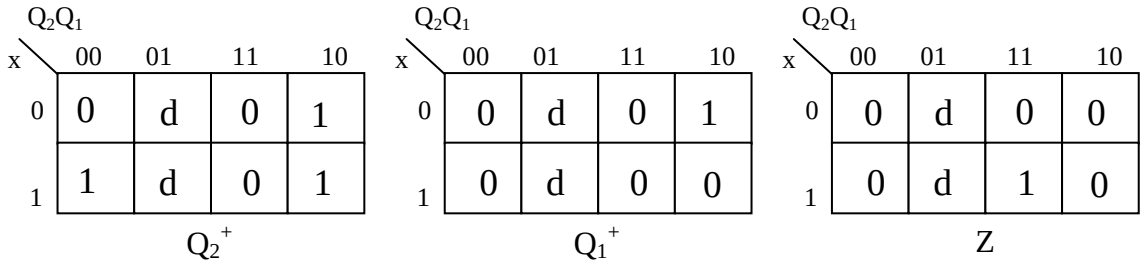


Figure 10.33 Next-state maps and output K-map.

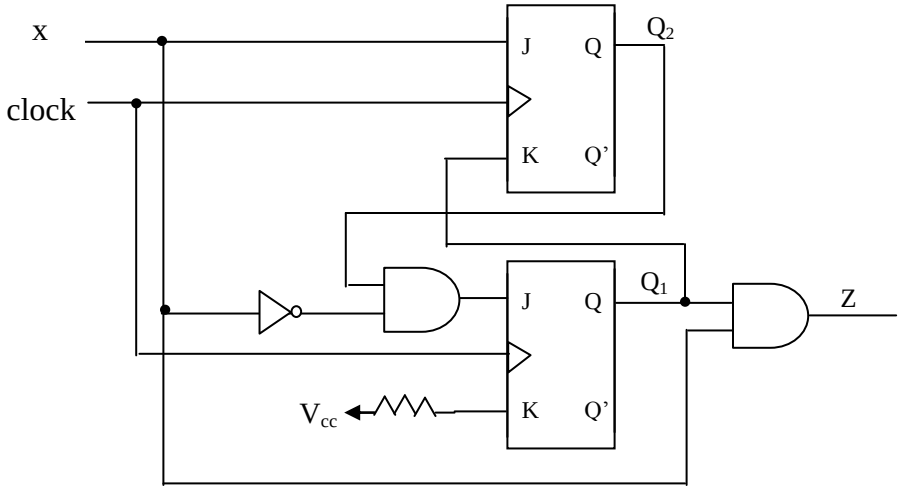


Figure 10.34 Sequential circuit of Mealy model to detect a sequence of 101.

Overlapping of Sequences

If overlapping is allowed in the detection of the sequence 101, the state diagrams for Moore model and Mealy model can be easily modified. For Moore model, state D represents the following situation. A sample input/output sequence for Moore model with consideration of overlapping is given in Table 10.19.

Table 10.19 Sample input/output sequence for a Moore model bit-sequence detector with overlapping.

Clock cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Input x	1	1	0	0	1	0	1	0	1	0	1	1	0	1	….
Output Z	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1

Condition D: All three bits, 101, have been detected. It is a state for the third bit of the sequence just detected and for the first bit of the next sequence.

Therefore, if the input x is 0 in state D, the first two bits of the next possible sequence, 10, have been detected. The next state should then be C. If the input x is 1 in state D, the second 1-bit of the previous sequence can be ignored because only one 1-bit is needed for the first bit of a new sequence. Thus the transition is from state D to state B. The modified state diagram for Moore model is given in Figure 10.35.

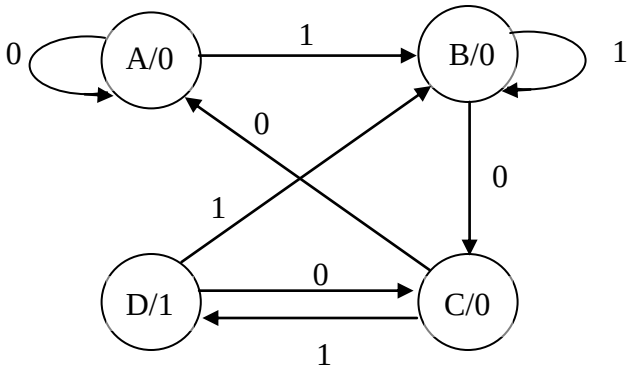


Figure 10.35 Moore model state diagram for overlapping sequences.

To modify the state diagram to allow overlapping for Mealy model, a sample input/output sequence is shown in Table 10.29. Condition C is explained below.

Condition C: The first two bits, 10, have been detected. If the present input x = 0, Z = 0. If x = 1, Z = 1. When x = 1, it also serves as the first bit of the next sequence and the next state is state B.

Table 10.20 Sample input/output sequence for a Mealy model bit-sequence detector with overlapping.

Clock cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Input x	1	1	0	0	1	0	1	0	1	0	1	1	0	1	….
Output Z	0	0	0	0	0	0	1	0	1	0	1	0	0	1	….

The modified state diagram is given in Figure 10.36.

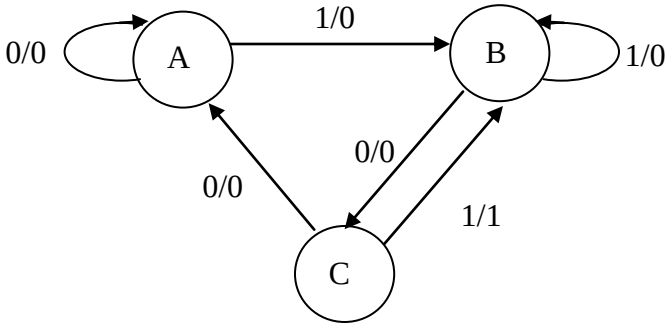


Figure 10.36 Mealy model state diagram for overlapping sequences.

PROBLEMS

1. Analyze the synchronous sequential circuit in Figure P10.1 using the following state assignment:

	Q_1Q_0
A:	0 0
B:	0 1
C:	1 1
D:	1 0

2. Repeat Problem 1 for the synchronous sequential circuit in Figure P10.2.

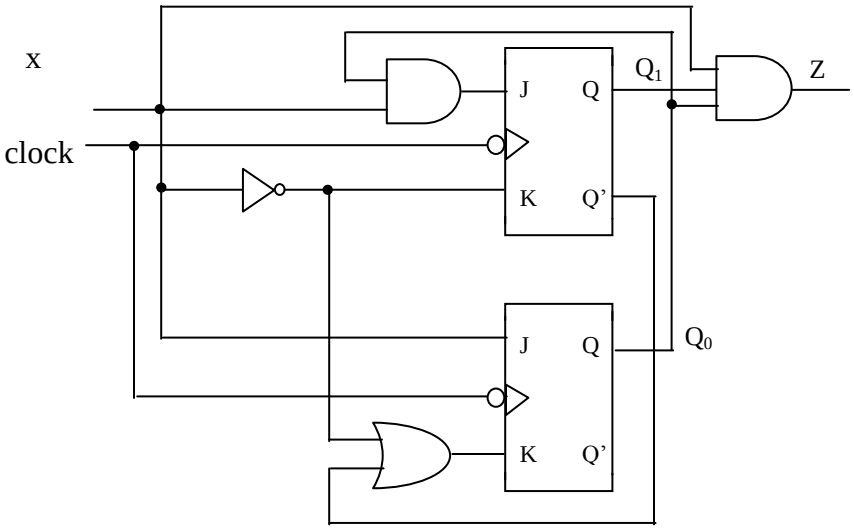
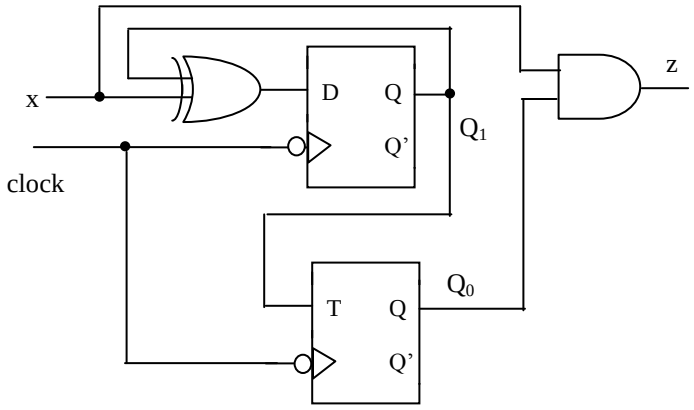


Figure P10.1

Figure P10.2



3. Given below are the excitation and output functions of a Moore model synchronous sequential circuit.

$J_1 = (xQ_0')'$ $K_1 = x + Q_0$ $T_0 = x\,Q_1 + x'Q_0$ $Z = Q_1\,Q_0'$

Analyze the synchronous sequential circuit.

4. Given below is the transition table for an 8-state counter known as Johnson counter. Realize the counter using D flip-flops.

$Q_0\,Q_1\,Q_2\,Q_3$	$Q_0^+\,Q_1^+\,Q_2^+\,Q_3^+$
0 0 0 0	1 0 0 0
0 0 0 1	0 0 0 0
0 0 1 1	0 0 0 1
0 1 1 1	0 0 1 1
1 0 0 0	1 1 0 0
1 1 0 0	1 1 1 0
1 1 1 0	1 1 1 1
1 1 1 1	0 1 1 1

5. Given below are the state table and state assignment for a synchronous sequential circuit. Realize the circuit using D flip-flops.

State assignment $Q_2\,Q_1Q_0$	Present state	Next State, output	
		x = 0	x = 1
0 0 0	A	B, 0	E, 0
0 0 1	B	A, 1	C, 1
0 1 0	C	B, 0	C, 1
0 1 1	D	C, 0	E, 0
1 0 0	E	D, 1	A, 0

6. Realize the following Moore model state table using (a) D flip-flops, (b) JK flip-flops.

State assignment Q_1Q_0	Present state	Next state		Output Z
		x = 0	x = 1	
0 0	A	B	C	0
0 1	B	B	C	1
1 1	C	A	D	0
1 0	D	A	D	1

7. Realize the following state table using (a) D flip-flops, (b) T flip-flops, and (c) JK flip-flops.

State assignment Q_1Q_0	Present state	Next state, output	
		x = 0	x = 1
0 0	A	A, 0	B, 0
0 1	B	C, 0	B, 0
1 1	C	D, 0	B, 0
1 0	D	B, 1	A, 0

8. Realize the following state table using JK flip-flops.

State assignment $Q_2\,Q_1Q_0$	Present state	Next State, output	
		x = 0	x = 1
0 0 0	A	B, 0	D, 0
1 0 1	B	A, 0	C, 1
1 0 0	C	D, 1	C, 0
0 0 1	D	B, 1	E, 1
0 1 0	E	C, 0	A, 0
1 1 0	F	E, 0	F, 1

9. Construct a state diagram for a synchronous sequential circuit that detects an input sequence of 1010. The output z is 1 when the sequence is detected. Otherwise z is 0. Sequences are allowed to overlap. A sample input/output is given below.

Input x 00101111010011101010100100
Output z 00000000000100000010100 0

10. Design a synchronous sequential circuit of Moore model that recognizes the input sequence 110. The output Z is 1 when the sequence is detected. Otherwise Z is 0. Use D flip-flops in the realization. A sample input/output is given below.

Input x 00101111010011001110010
Output z 00000000010000010000100

11. Design the bit-sequence recognizer in Problem 10 as a Mealy model machine.

12. Design a synchronous sequential circuit of Moore model that recognizes the input sequence 1100. When the sequence is detected, the output z becomes 1. z will return to 0 after two consecutive 1's are detected. The circuit will then start the detection of the next 1100 sequence. Use T flip-flops. A sample input/output sequence is given below.

Input x	00101100101101001100111001 0
Output z	00000000111100000000011000000