Dr. Yan Luo's Curriculum Vitae

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1. CONTACT

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2. EDUCATION

Ph.D. in Computer Science	University of California Riverside, July 2005
Thesis: *Performance Evaluation and Low Power Design of Network Processors* Advisors: Dr. Laxmi Bhuyan and Dr. Jun Yang	
M.E. in Computer Science and Engineering	Huazhong University of Science and Technology, China, June 2000
B.E. in Computer Science and Engineering	Huazhong University of Science and Technology, China, June 1996

3. RESEARCH

- Network processors
- Low-power microprocessor architecture
- Internet router and web server architectures
- Parallel and distributed processing
- Embedded systems
- Simulation and performance evaluation

4. PROFESSIONAL EXPERIENCE

- **August 2005 - present, Assistant Professor, University of Massachusetts Lowell**
  Teach undergraduate and graduate courses in computer engineering. Conduct research on network processors, low power microprocessor, multiprocessor router architecture, parallel and distributed processing etc.
- **2001 - 2005, Graduate Student Researcher, University of California, Riverside**

Researched on network processors, low power microprocessor, multiprocessor router architecture, parallel and distributed processing, and design verification. Built the first open-source cycle-accurate simulator of network processors with power evaluation framework. Experimented power efficient techniques for network processors. Developed Intel IXP2400 based content-aware web switch. Developed software APIs and device drivers to offload protocol processing on NPs. Studied multiprocessor shared memory Internet routers.

- **2000 - 2005, Teaching Assistant, University of California, Riverside**
  Taught a variety of computer science courses at undergraduate level. Planed and prepared laboratory topics and materials. Conducted lecturing in laboratories. Substituted lectures in classroom for instructors. Courses taught: Computer Architecture Laboratory, Design and Architecture of Computer Systems, Advanced Computer Architecture, Design of Operating Systems, Concurrent Programming and Parallel Systems, Introduction to Computer Science (C++ programming).
- **1997 - 2000, Research Assistant, Huazhong University of Science and Technology**
  Conducted research on cluster computing and real-time systems. Implemented clock synchronization in a cluster environment. Proposed bandwidth allocation algorithms for real-time communication.
- **1996 - 1997, IT Engineer, R & D, Guangdong Nortel, China**
  Conducted various system administration and software development support in full-time. Designed and supported a web-based Problem Reporting System. Administered UNIX/PC/MAC systems. Assisted telecom switch hardware and software testing.

5. PUBLICATIONS

5.1. Journal Papers

Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan, Conserving Network Processor Power Consumption By Exploiting Traffic Variability, accepted by and to appear in *ACM Transactions on Architecture and Code Optimization.*.

L. Zhao, Y. Luo, L. Bhuyan, R. Iyer, A Network Processor Based Content Aware Switch, *IEEE Micro Special Issue on High-Performance Interconnects,* Volume 26, No. 3, pp. 72-84, May/June 2006

Yan Luo, Jun Yang, Laxmi Bhuyan, Li Zhao, NePSim: A Network Processor Simulator with Power Evaluation Framework, *IEEE Micro Special Issue on Network Processors for Future High-End Systems and Applications, Sept/Oct 2004.*

Yan Luo, Laxmi Bhuyan, Xi Chen, Shared Memory Multiprocessor Architectures for Software IP Routers, *IEEE Transactions on Parallel and Distributed Systems*, Vol 14, No.

12, Dec 2003

Xi Chen, Yan Luo, Harry Hsieh, Laxmi Bhuyan and Felice Balarin, Assertion-Based Verification and Analysis of Network Processor Architectures, to appear, *International Journal of Design Automation for Embedded Systems*, Kluwer Academic Publishers.

Jia Yu, Jun Yang, Shaojie Chen, Yan Luo, Laxmi Bhuyan, Enhancing Network Processor Simulation Speed with Statistical Input Sampling, *Lecture Notes in Computer Science*, Volume 3793, Oct 2005, Pages 68 - 83, Springer-Verlag Publishers

5.2. Conference Papers

Piti Piyachon, Yan Luo, Efficient Memory Utilization on Network Processors for Deep Packet Inspection, under review.

Jingnan Yao, Yan Luo, Laxmi Bhuyan, Ravi Iyer, Optimal Network Processor Topologies for Efficient Packet Processing, *IEEE Globecom 2005, St Louis, MO, Nov 28-Dec 2, 2005*

Li Zhao, Yan Luo, Laxmi Bhuyan, Ravi Iyer, SpliceNP: A TCP Splicer using A Network Processors, *ACM Symposium on Architectures for Network and Communication Systems, Princeton, NJ, Oct 26-28, 2005*

Li Zhao, Yan Luo, Laxmi Bhuyan, Ravi Iyer, Implementation and Design of A Content-aware Switch Using A Network Processor, *IEEE Hot-Interconnect, Stanford, CA, August 2005*

Yan Luo, Jia Yu, Jun Yang, Laxmi Bhuyan, Low Power Network Processor Design Using Clock Gating, *IEEE/ACM Design Automation Conference (DAC), Ahaheim, California, June 13-17, 2005*

Xi Chen, Yan Luo, Harry Hsieh, Laxmi Bhuyan, Felice Balarin, Utilizing Formal Assertions for System Design of Network Processors, Design Forum, *Design Automation and Test in Europe (DATE)*, 2004.

Yan Luo, Li Zhao, Laxmi Bhuyan, Walid Najjar, Evaluating the Impact of Architectural Features on Communication Benchmarks, *Communications in Computing*, Nevada, USA, June 24-27, 2002

David Watson, Yan Luo, and Brett Fleisch, Experiences with Oasis+: A Fault Tolerant Storage System, *Proceedings of the IEEE International Conference on Cluster Computing*, Oct 8-11 2001, Newport Beach, CA.

David Watson, Yan Luo, and Brett Fleisch, The Oasis+ Dependable Distributed Storage System, *Proceedings of the 2000 Pacific Rim International Symposium on Dependable*

Computing, December 18-19, 2000, Los Angeles, CA.

6. FUNDING

Distributed Packet Inspection using Network Processors	Intel Corporation, PI, 2006-
ACM ANCS Travel Grant	ACM, Nov 2005

7. HONORS

Chancellor's Distinguished Fellowship	University of California Riverside, 2000 - 2005
Excellent Employee Award	Guangdong Nortel, China, 1997
Outstanding Student Award	Huazhong University of Science and Technology, China, 1992 - 1996

8. SERVICES

Co-chair of UML-ADI National DSP Contest 2006

Program Committee of the IEEE International Workshop on Multimedia Technology and Ubiquitous Computing (MTUC 2006), Taichung, Taiwan, June 5-7, 2006

Referee for IEEE Transaction on Computers, IEEE Micro, Journal of System Architecture, IPDPS'04, ICPP'04, BEACON'04, DAC'05, Infocom 2006, IEE Computer and Digital Techniques, ACM TACO

9. PROFESSIONAL AFFILIATIONS

Member of IEEE and ACM