CHAPTER 6

NANOWIRE ASSEMBLY AND INTEGRATION

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Semiconducting, metallic and insulating nanowires are attractive building blocks in nanotechnology due to their small size and anisotropy. Moreover, it is possible to fabricate homogeneous or heterogeneous nanowires with high purity and crystallinity in a parallel and cost effective manner. Strategies have also emerged to position nanowires precisely on substrates to allow integration of nanoelectronic devices. In this chapter, we describe the fabrication and assembly of nanowires to form functional devices. Several fabrication strategies including vapor-liquid-solid (VLS) and electrodeposition in nanoporous templates are discussed. We detail advances made in the bottom-up integration of nanowires using patterned growth and directed assembly. Finally, some functional devices fabricated using nanowires are reviewed, and strategies to reduce errors and improve defect tolerance are discussed.

Keywords: Nanowire (NW); Nanotechnology; Self-assembly; Nano-soldering; Nanoelectronics; Directed assembly; Interconnects; Bottom-up assembly.

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1. Introduction

A nanowire is a nanoparticle whose diameter is much smaller than its length. Nanowires typically have diameters of 10-100 nm or less and lengths of 100 nm to tens of microns. Nanowires can be fabricated out of a wide range of materials including both inorganic and organic electrical conductors, semiconductors and insulators [1–13]. In contrast to other nanoparticle shapes such as polyhedra, rods and spheres, nanowires are long (length >> diameter); this length facilitates relatively easy integration with patterned micro and sub-micron device architectures. The high anisotropy in the properties of nanowires can also be an advantage in facilitating the propagation of electricity and light in specific spatial directions. Nanowires can also be fabricated with multiple heterogeneous segments, spaced precisely along the length of the nanowires. Nanowires have been fabricated of single crystal or amorphous materials, using a variety of methods. Functional devices such as diodes have also been fabricated within a single nanowire [14].

While a single nanowire device is itself a useful component, when positioned precisely on substrates, or when integrated with other nanowires, can result in integrated functional devices. Hence, the nanowire is often treated as a building

block that will be used to construct nanoelectronic, nanophotonic and nanofluidic devices. The idea of using building blocks to fabricate and integrate functional devices from the bottom-up is motivated by the fact that in recent years, the conventional lithographic scaling down of microelectronic, photonic and microelectromechanical systems (MEMS) to the 50–500 nm length scale has encountered severe challenges in the cost-effective, mass production of devices and integrated systems. Hence, there is an increasing need to develop new nano-fabrication technologies to address the challenges of decreasing dimensions, in order to enable the era of nanotechnology.

In this chapter, we review methods to integrate nanowires with each other and with substrates with the end goal of fabricating functional devices from the bottom-up. We will first review non-lithographic methods commonly employed to fabricate nanowires in a cost-effective and parallel manner. We will then discuss some approaches to assemble nanowires into integrated structures and devices. Finally, we will introduce several representative applications of integrated nanowire structures and devices, and some perspectives in the future assembly and integration of products and devices based on nanowires.

2. Nanowire (NW) Fabrication

Several non-lithographic methods are available to fabricate nanowires. The methods usually involve the spontaneous or templated growth of the nanowire using vapor or solution phase chemical reactions. In all cases, growth of the nanowire is directed preferentially along its long axis using chemical (e.g. a catalyst or surfactant) or physical (e.g. a porous membrane) methods. These methods are described below.

2.1. *Vapor-liquid-solid (VLS) method*

The vapor-liquid-solid (VLS) method for growing nanowires involves the chemical reaction between gaseous reactants and a liquid or molten catalyst to form nanowires on a solid substrate. VLS is the most attractive method for growing high purity, single crystal nanowires. As can be seen in Fig. 1(a), the three stages in the VLS growth mechanism are alloying, nucleation and axial growth [15]. The nanowires produced generally have alloy droplets on their tips. The example shown in Fig. 1(b) typifies the process which includes a solid catalyst that forms an alloy with a gaseous reactant at elevated temperatures. The alloy then becomes supersaturated with the reactant, which causes nucleation of the nanowire and preferential axial precipitation (growth) of the nanowire from the liquid alloy surface. Using this process, single crystal nanowires composed of silicon, germanium, ZnO, GaN, and SnO_2 have been fabricated [15–22]. Core-shell nanowires can also be fabricated by this method [23]. Other similar techniques, such as supercritical fluid-liquid-solid (SFLS) or supercritical fluid-solid-solid (SFSS) [24-26], and solution-liquid-solid (SLS) [27,28] methods have also been used to fabricate Si, Germanium, and CdSe nanowires.

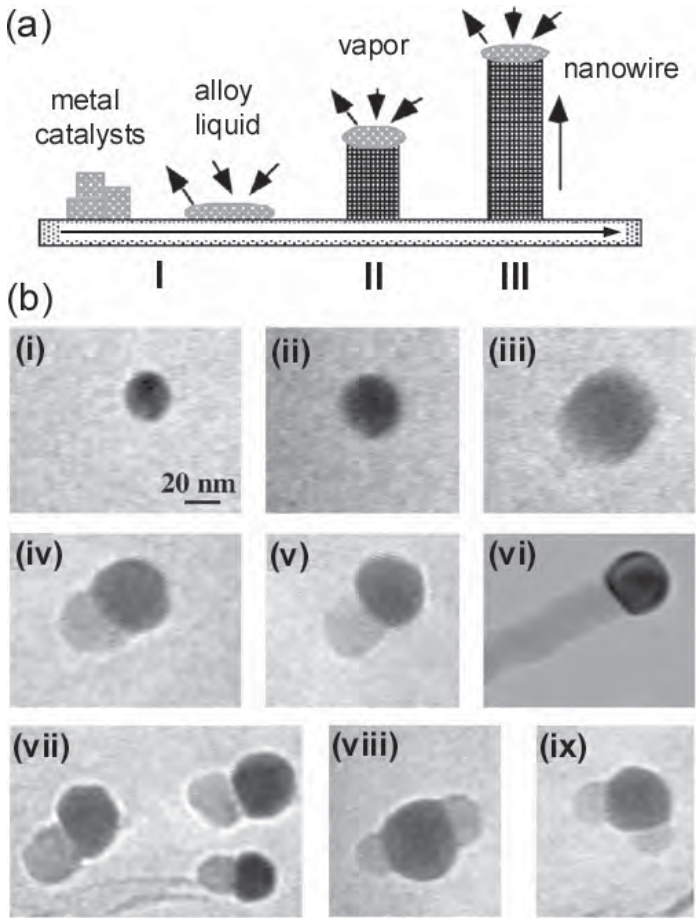

Figure 1. (a) Schematic of vapor-liquid-solid (VLS) germanium (Ge) nanowire growth mechanism including three stages (I) alloying, (II) nucleation, and (III) axial growth. (b) *In situ* TEM images recorded during the process of Ge nanowire growth. (i) Au nanoclusters in solid state at 500°C; (ii) alloying initiates at 800°C, at this stage Au exists in mostly solid state; (iii) liquid Au/Ge alloy; (iv) the nucleation of Ge nanocrystal on the alloy surface; (v) Ge nanocrystal elongates with further Ge condensation and eventually a wire forms (vi). (vii) Several other examples of Ge nanowire nucleation, (viii, ix) TEM images showing two nucleation events on single alloy droplet. Reprinted with permission from [15] by American Chemical Society.

2.2. *Solution phase synthesis*

This process involves the formation of nanowires from a liquid precursor, usually in the presence of a catalyst or molecular template [29–33]. One common example is the reduction of silver or gold salts in the presence of polymers or surfactants such as polyvinylpyrrolidone (PVP) or cetyltrimethylammonium bromide (CTAB). The surfactants adsorb preferentially on specific crystalline faces and enhance or inhibit growth along those faces, thereby resulting in the spontaneous growth of nanowires (along the planes in which growth is preferred). In certain cases, solid crystalline seeds are also added to the solution, to initiate preferential axial growth along specific crystal faces. As an example, gold nanorods were prepared by the addition of ∼4 nm gold nanospheres as seeds and the subsequent reduction of metal salt with

a weak reducing agent (ascorbic acid) in the presence of a surfactant to produce nanorods. By adding another component such as ascorbic acid, metal was preferentially deposited at the ends of the rods to from Dog-bone like nanowires [34]. In solution, a variety of parameters such as temperature, concentrations and surfactants can be varied to gain some control over the type of nanowires formed.

2.3. *Electrodeposition in nanoporous templates*

This method employs physical templates to direct the growth of nanowires within nanoporous membranes [35–41]. Nanoporous membranes are fabricated using track etching or anodic electrochemical methods; these membranes are also commercially available with pore sizes ranging from 15 nm to 500 nm and membrane thickness up to 60 μm. Briefly the process (Fig. 2[a]) involves sealing one face of the membrane with a conductive seed layer. This seed layer is usually deposited onto the membrane using thermal or sputter evaporation. Single segment or multisegmented nanowires are then deposited in the membrane using an electrolytic solution containing the appropriate ions. The seed layer and a counter electrode immersed in the solution form the electrolytic cell. The length of the segments within the nanowires is restricted by controlling the current density or voltage, and the duration of electrodeposition process. Electrodeposition in templates is the most attractive method to fabricate nanowires with multiple segments (Fig. 2[b]) and theoretically can be used to fabricate nanowires composed of any material that can be electrodeposited.

2.4. *Electrospinning*

Electrospinning is a simple and efficient way to produce polymeric nanowires, also called nanofibers. The basic set-up utilizes a syringe through which polymer

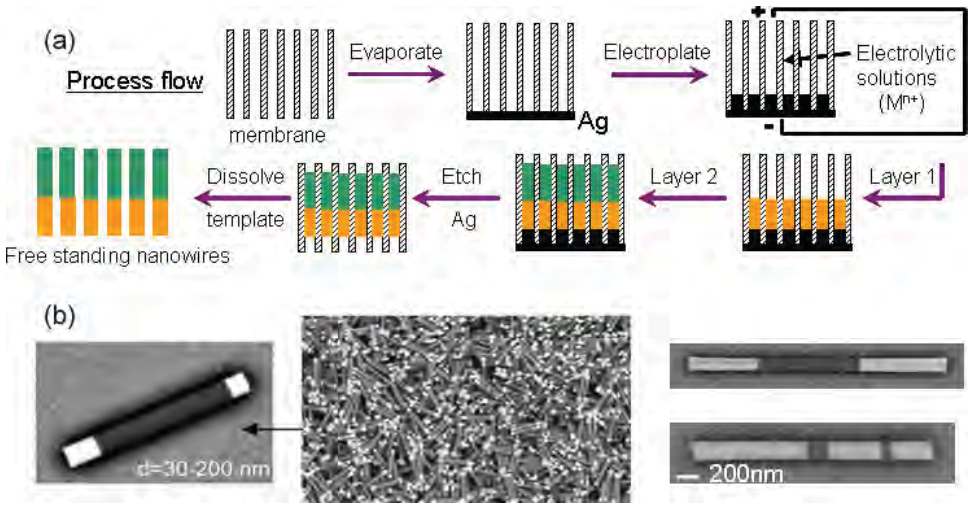

Figure 2. (a) Schematic of nanowire fabrication process using electrodeposition in nanoporous templates. (b) several examples of fabricated multisegment nanowires.

solutions are driven; their surface tension at the tip, under high electric field, can be overcome resulting in the ejection of a charged jet. The electrical forces elongate the jet thousands or even millions of times and the jet becomes very thin, down to nanoscale. After the solvent evaporates, or the melt solidifies, long polymeric nanofibers can be collected on an electrically grounded metal sheet. As compared to other fabrication methods, electrospinning facilitates the formation of extremely long nanowires with well controlled curvature [42–49].

There are other non-lithographic methods that are used to fabricate nanowires including laser ablation and directed growth along step edges or crystal planes [50]. Nanowires can also be fabricated by stringing together particles using dielectrophoresis or biomolecules (viruses) [51–54]. In all cases however the anisotropic growth of the nanowire occurs as a result of preferential growth of a material along one axis.

3. Nanowire (NW) Assembly and Manipulation

Although it is possible to manipulate and position nanowires using nanoscale tools such as scanning probe microscopes [55], these processes are serial, slow and expensive. Hence, strategies need to be developed either to directly integrate the growth of nanowires to form the final device, or to assemble nanowires into functional devices. These strategies or processes need to be highly efficient (high speed and low cost), in order to enable a manufacturable nanoscale process.

3.1. *Controlled or patterned growth*

Since a number of processes used to grow nanowires involve a catalyst or a template, it is conceivable that by patterning the catalyst or template directly on a substrate, it will be possible to grow the nanowires at specific spatial locations so that they grow out of the substrates in specific directions (see Fig. 3[a–b]) [56–72]. This is an attractive strategy that has been explored to form nanoscale vertical or horizontal interconnects. In these cases, the growth of the nanowires occurs between two patterned microstructures and in doing so, the nanowires electrically connect with the substrates (see Fig. 3[c–e]).

3.2. *Self-assembly and directed assembly*

Recently, the strategy of directed assembly has emerged as a highly parallel, cost-effective fabrication methodology that is capable of generating fully 3D structures and integrated systems. Directed assembly of engineered structures is inspired by biological self-assembly; nature is able to mass produce a wide variety of complex 2D and 3D structures with sizes ranging from the sub-nanometer to the millimeter and beyond [73–77]. This methodology involves tumbling chemically patterned components in a fluidic medium, so that they can interact with each other, and form

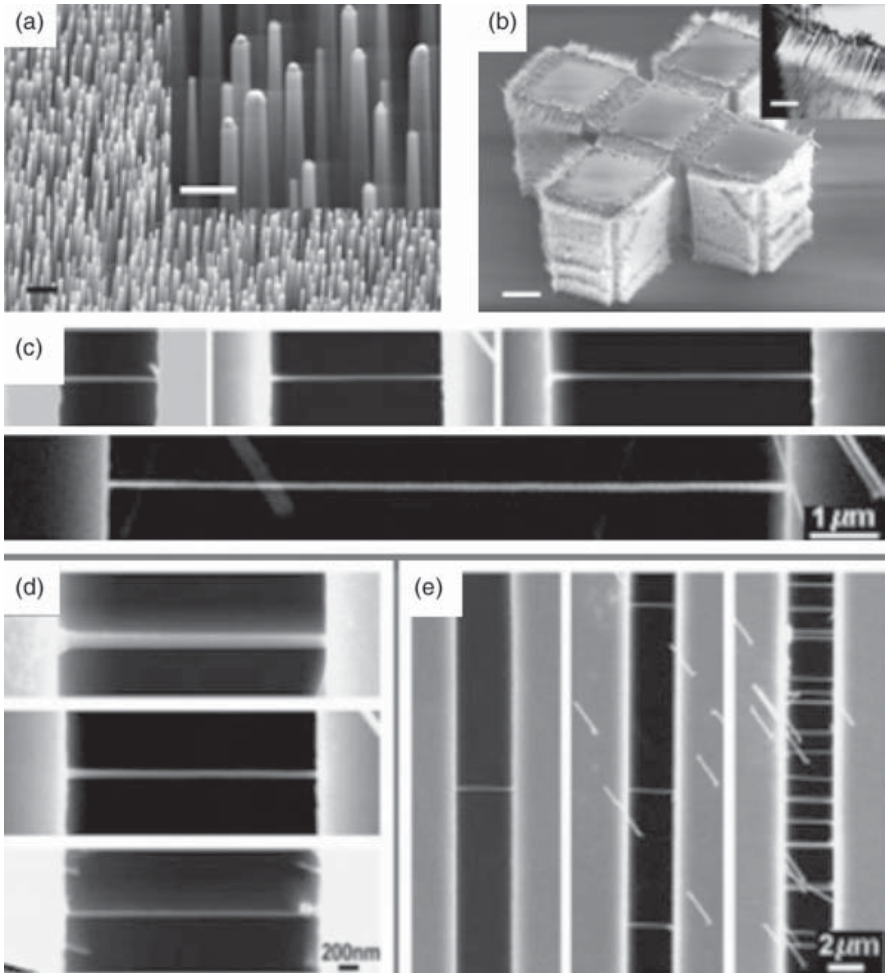

Figure 3. (a) SEM images of vertically aligned Si nanowire arrays grown from Au clusters deposited on Si(111) substrates. Scale bar is 30 nm (b) Laterally aligned Si nanowire arrays grown on Si pillars bounded by (111) sidewalls fabricated on (110) silicon-on-insulator (SOI) substrates. (a) and (b) reprinted with permission from [71] by American Chemical Society. (c) (d) and (e) Control of length (c), diameter (d) and density (e) of Si nanowires in microtrenches. Reprinted with permission from [64] by Wiley.

stable structures with precise function. The chemical patterning of components is engineered using a variety of forces that direct the orientation and binding of the components. This manufacturing paradigm has been largely unexplored in human engineering since the process is generally perceived to be indeterministic and uncontrollable. There are several strategies that have been explored in the past decade to direct the assembly of nanowires with each other and with substrates. We now review some of these strategies.

3.2.1. *Molecular/Bio-molecular linkers*

It is possible to direct the assembly of nanowires using molecular linkers that form chemical bonds with each other. The molecular linkers are first attached to the

nanowires by exposing the nanowires to them (either in solution or vapor phase). Since there are a large variety of molecules that specifically bind to each other such as ligands and receptors, it is possible to incorporate a high degree of specificity to the assembly process. Several groups have also utilized biological molecules such as proteins, DNA, and even viruses to link nanoparticles together in complex architectures [78–86]. The advantage of using biological molecules to direct assembly is that they exhibit complex architectures that facilitate lock-key based recognition, cooperativity and hierarchy.

3.2.2. *Electrical field-assisted assembly (including DEP)*

Dielectrophoresis (DEP) is the motion of neutral particles under the influence of an external non-uniform electric field [87]. DEP arises when the neutral particles get polarized and experience different forces at the ends of the polarized dipole as a result of the non-uniform electric field experienced at these ends. The difference tends to force the polarized particles into regions of differing field strength. Pohl [87] outlines the case of a cylinder of radius a and length L; the force experienced (assuming the cylinder is initially at right angles to the applied field) can be approximated as,

$$F_{\text{cylinder}} = \pi a^2 L \frac{\varepsilon_1[\varepsilon_2 - \varepsilon_1]}{\varepsilon_2 + \varepsilon_1} \nabla |E|^2$$

where E is the magnitude of the field and ε_2 and ε_1 are the dielectric constants of the cylinder and medium, respectively. DEP requires relatively high field strengths and this required field strength depends on the difference in dielectric constant between the particle and medium in which DEP is being carried out. In media of low dielectric constant ($\varepsilon = 2-7$) this is of the order 10^4 V/m, whereas in media of high dielectric constant (water, $\varepsilon \sim 80$) lower fields (500 V/m) are adequate. These fields are easily achievable in microscale gaps even at small voltages, due to high field strengths and can be used to direct the assembly of nanowires. The nanowires are typically suspended in a solvent over contact pads across which a voltage is applied. The nanowires then move, experiencing a force that causes them to orient on the substrates relative to the contact pads. By changing the solvent, aspect ratio of the nanowires, geometry and spacing between the electrodes, and the frequency and field strength it is possible to direct both reversible and irreversible assembly of nanowires in a variety of architectures (Fig. 4) [88–98]. The advantages of DEP are that the strategy can be scaled to the wafer level, such that the nanowires can be incorporated in parallel into many devices, with control over both placement and alignment.

3.2.3. *Magnetic assembly*

Magnetic force is another interaction that can be utilized to assemble and integrate nanowires. In order to facilitate magnetic assembly, either segments within

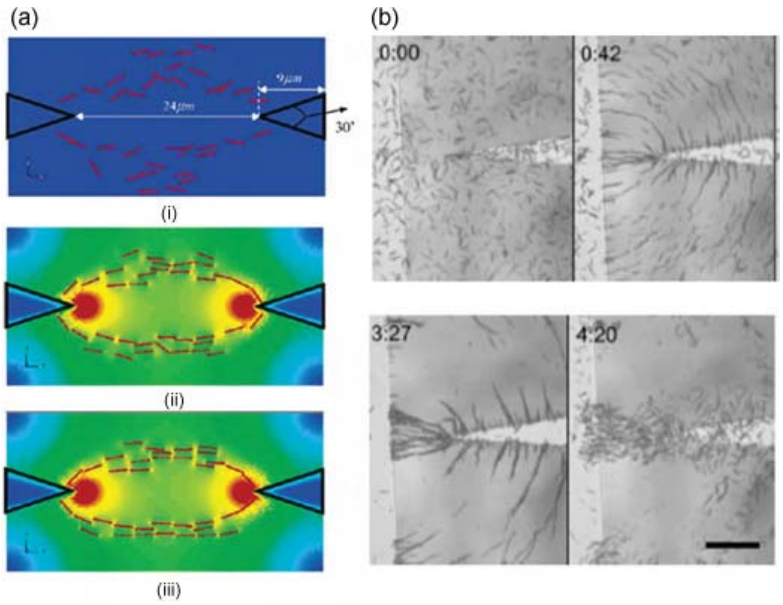

Figure 4. (a) Sequential images of nanowires lining up between triangular-shaped electrodes (angle: 30°). AC field of 5 MHz (0.5V/μm) is applied between electrodes. (i) $t = 0$ s; (ii) $t = 0.5$ s; (iii) $t = 1.0$ s. Reprinted with permission from [96] by American Chemical Society. (b) Reversible silver (Ag) nanowire network formation from a suspension in water, with DEP at 0.2 V and 100 kHz. The frames are labeled with the time (min:s) after the first frame. The first frame is taken just before initiation of DEP, and the third frame is taken just before ending DEP. The scale bar corresponds to 30 μm. Reprinted with permission from [95] by American Institute of Physics.

the nanowire or the entire nanowire itself is constructed from ferromagnetic constituents such as nickel, iron, cobalt or alloys. When magnetized, these segments act like small magnets and orient themselves in an external magnetic field such that the energy is minimized. The nanowires interact with each other and with magnetic substrates such that they assemble into bundles and end to end networks [99–106]. Magnetic forces can also be used to precisely position nanowires on substrates.

3.2.4. *Holographic optical traps*

In this approach, nanowires are dispersed in a fluidic medium on the stage of a light microscope and manipulated by either single or multiple diffraction-limited-optical traps using a holographic optical tweezer. Optical tweezers utilize focused laser beams to apply a radiation force on particles, in order to trap and manipulate them. Optical traps are attractive for nanowire assembly since they can be used to manipulate nanowires in closed chambers with high spatial accuracy (<1 nm); they also are applicable to a wide range of materials. While manipulation with a single optical beam is a serial process, recently *Grier's* group has demonstrated that holographically projected arrays of optical traps can be used to manipulate nanowires in parallel and that semiconductor nanowires can even be rotated, cut and fused to assemble complex structures in 3D using holographic optical traps [107,108].

3.2.5. *Langmuir-Blodgett technique*

The Langmuir-Blodgett method uses the compression of nanowires (capped with surfactants) at a liquid interface, followed by transfer onto solid substrates. Nanowires, capped with surfactants are first dispersed in a fluidic medium, the surfactants cause the wires to float at the fluid-air interface. Solid barriers surrounding the nanowires are made to approach each other in a highly precise and well-controlled manner; the barriers compress the nanowires at the interface causing them to rotate, align and form closed packed ordered arrays. The main highlight of this technique is that it is possible to form ordered arrays of nanowires as large as tens of centimeters in a relatively straightforward manner [109–114].

3.2.6. *Surface tension (capillary forces) based assembly*

Although the aforementioned strategies have been very successful in directing the assembly of nanowires into 2D and 3D integrated structures, in many cases, the structures formed are not permanently bonded to one another, i.e. the assemblies although held together in the fluidic medium in which they are assembled, fall apart when taken out of the medium or during mild sonication. Additionally, in directed assembly between rigid nanocomponents, the strength and the extent of binding is proportional to the overlap area at the binding site between components. Any local roughness of the components (especially when the size approaches 100 nm) reduces the effective binding contact area due to asperities, and consequently decreases the strength and extent of binding. Hence, assemblies often consist of only a few bonded nanocomponents, and large scale integration is extremely challenging. It should be noted that in biological self-assembly, most of the components utilized in the assemblies are soft and deformable which allows the mating surfaces to conform to one another resulting in large contact areas for optimum binding.

Surface tension based assembly involves (i) modification of the surface energy of specific segments of the nanowires using *hydrophobic* organic molecules that attached preferentially to specific segments, (ii) precipitation of a *hydrophobic* or *hydrophilic* liquid layer on the modified segments, and (iii) agitation of the nanowires in a *hydrophilic* or *hydrophobic* medium to facilitate favorable interactions between nanowires, and direct the assembly process. When nanowires patterned with *hydrophobic* liquid layers collide with one another in a hydrophilic liquid, there is a tendency of the liquid layers on different nanowires to fuse with one another on contact, in order to minimize their surface free energy. This surface tension force between liquid layers on colliding nanowires is large enough to hold the wires together in the liquid [115,116]. Since this kind of assembly involved binding between liquid layers (that are soft and deformable) patterned on the nanowires, the roughness of the nanowires does not hamper binding and it is possible to accomplish large scale integration. By patterning different hydrophilic and hydrophobic

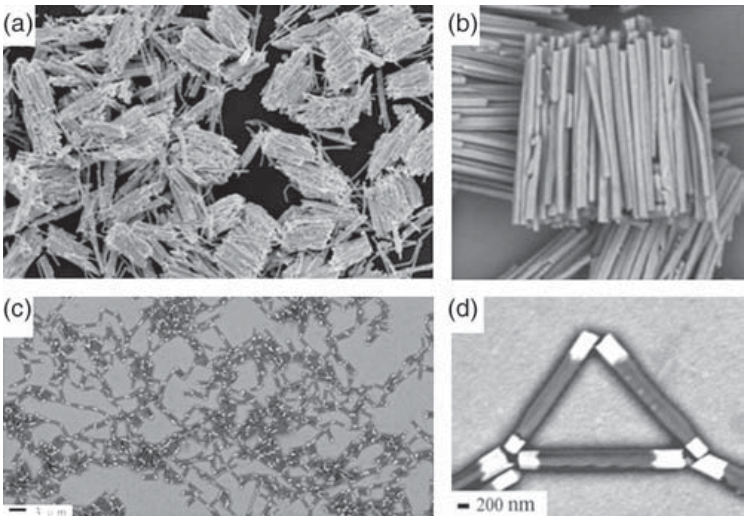

Figure 5. SEM images of (a) and (b) large-scale three-dimensional (3D) Au nanowire bundles bonded by polymeric adhesive. SEM images of (c) large-scale 2D Au-nickel (Ni)-Au nanowire networks and (d) a triangle structure showing end-to-end nanowire connection. (a) Reprinted with permission from [116] by The Minerals, Metals & Materials Society, and (b–d) reprinted with permission from [115] by American Chemical Society.

segments on the nanowire, and precipitating a polymerizable adhesive, it is possible to direct the assembly of nanowires into permanently bonded bundles or 2D end-to-end networks (see Fig. 5).

4. Nanowire (NW) Integration

In order to fabricate a functional device using nanowires, it is often necessary to integrate the nanowires with other components such as contact pads and silicon substrates. It is important to note that although nanoscale components are attractive because their small size facilitates higher packing densities and enhanced functionality, actual devices tend to be on the macroscale (i.e. the scale of the human world). It is thus necessary to interface nanoscale components with micro and finally macroscale components in a hierarchical manner, so that the devices may be functional on the macroscale.

The semiconductor industry has utilized a top-down lithographic approach using patterning, etching, thin film deposition and polishing to fabricate devices with nanowires [117]. In this chapter we do not review this top-down approach, but will mention that there are limitations in terms of the cost-effective, parallel fabrication of devices with nanowires.

There are numerous strategies to integrate nanowires with microfabricated contact pads from the bottom-up. These involve direct growth, imprinting or directed assembly. For electrical devices, after assembly it is often necessary to form a robust electrical contact. When gold contacts are used, this can be done by annealing as gold diffuses relatively easily. However, for other materials this may not be possible.

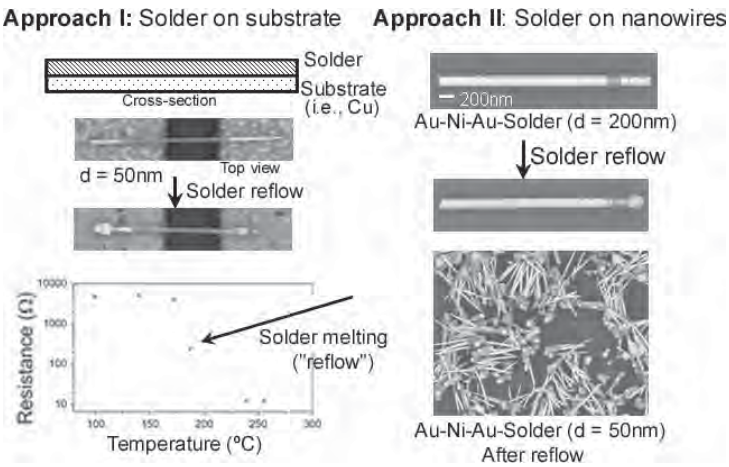

Figure 6. Schematic and SEM images showing two approaches to enable nanoscale soldering. SEM images are reprinted with permission from [105] by the Institute of Electrical and Electronics Engineers, Inc., from [116] by The Minerals, Metals & Materials Society, and from [118] by Wiley.

Our group has focused on investigating and developing the use of solder (low melting point metal or metal alloy) on the nanoscale to form electrical contacts. Soldering technology is one of the most widely used and dominant methods for microelectronics and device integration. Basically our strategy involves the fabrication of nanowires with solder deposited in regions where a robust electrical contact is needed. Figure 6 shows two basic approaches that can be used to solder nanowires to substrates and with each other to form electrically interconnected ordered structures or devices. The first approach is to directly put nanoscale solder onto the substrate, normally through electrodeposition, and then integrate (solder) functional nanowires onto the substrate to form robust electrical contact. Another approach is to fabricate nanoscale solder segments directly onto nanowires, and then solder them at the desired location. Solder reflow (melting) can be carried out in an inert atmosphere to bond nanowires to substrates or to each other, and it may even be

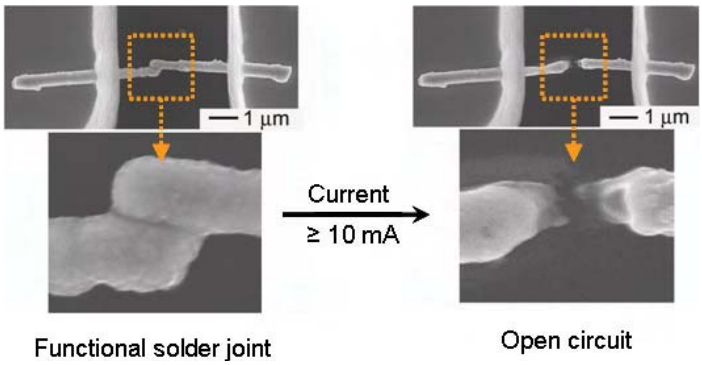

Figure 7. SEM images of contact pads patterned on top of fused nanowires, connected by a solder joint, before (left) electrical testing and after (right) applying a current of approximately 10 mA across the contact pads. The high current caused a break between the nanowires and resulted in an open circuit. Reprinted with permission from [118] by Wiley.

done in a fluidic medium [105,116,118]. When a high current is applied to a functional (electrically-conductive) solder joint, the local heat effect breaks the solder joint resulting in an open circuit (electrically non-conductive), thereby acting as a nanoscale "fuse" (see Fig. 7). These features of nanoscale soldering can be utilized to integrate nanowires into practical devices. As compared to macroscale soldering, however, extra care must be taken to minimize corrosion, diffusion and oxidation of the solder segments during the process.

5. Nanowire (NW) Applications

5.1. *Diodes and field effect transistors (FET)*

Homogeneous semiconducting nanowires have been used as the active semiconductor material and have been integrated within field effect transistor stacks. Since semiconducting nanowires are naturally thin (as well as single crystalline), they eliminate the need for patterning of the active semiconductor layer in these devices. However, considerable lithography is required to integrate these semiconducting nanowires within devices. Recently, the fabrication of nanowire heterostructures has allowed the inclusion of semiconductors, dielectrics and metals within the same nanowire. Park *et al* have fabricated nanowire diodes by electrodepositing segmented nanowires composed of Au-polypyrrole (Ppy)-Cadmium (Cd)-Au [14]. In this case, the nanowire contains the semiconductor and metallic constituents within the same nanowire. Current voltage (I-V) measurements on devices constructed from single Au-Ppy-Cd-Au rods exhibited diode behavior at room temperature (see Fig. 8(a)) [14]. Kovtyukhova *et al* have fabricated nanowires containing semiconducting, metallic as well as insulators to fabricate nanowire transistors [119]. These nanowires composed of metallic Au source and drain electrodes, the CdS (Se) semiconductor and the SiO_2 gate dielectric. The coaxially gated in-wire CdS and CdSe nanowire transistors were fabricated in nanoporous templates using a combination

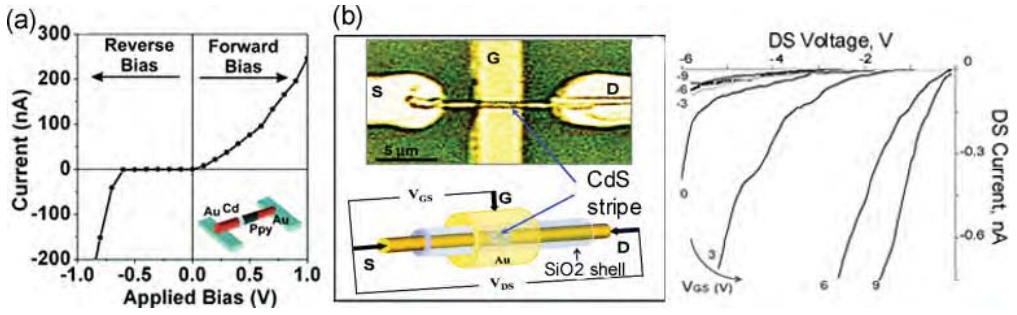

Figure 8. (a) I-V characteristics of a single Au-polypyrrole (Ppy)-cadmium (Cd)-Au nanowire at room temperature. Reprinted with permission from [14] by American Chemical Society. (b) Optical micrograph and schematic drawing of the test structure and a Au/CdS/Au@(SiO_2) nanowire aligned for measurement of electrical properties. Letters S, D and G indicate source, drain and gate electrodes, respectively. The curve shows typical $I_{DS} - V_{DS}$ characteristics of in-wire TFTs for different values of gate voltage (V_{GS}). Reprinted with permission from [119] by American Chemical Society.

of surface sol-gel and electrochemical deposition techniques (Fig. 8(b)). The I-V characteristics of the devices showed a field effect, which was more pronounced at negative drain voltages (See Fig. 8(b)). Other efforts have also been made to fabricate nanowire-based diodes and field-effect-transistors [120–124].

5.2. *Sensors*

Since the diameters of nanowires are small and often comparable to the size of biological and chemical species being sensed, their properties are often dramatically affected on adsorption of certain analytes [125–127]. The electronically switchable properties of semiconductor nanowires offer the possibility for a direct and label-free electronic readout. Sensors with changes in electronic responses are attractive since they can be readily used to trigger alarms, LEDs, readouts etc. *Lieber's* group has pioneered the use of semiconducting nanowires for sensing using a field effect transistor (FET) configuration [128–131]. In the FET, the semiconducting nanowire (with a diameter as small as 2 nm) is placed on top of a gate dielectric (and gate) and bridges source and drain electrodes. The one dimensional morphology of the nanowire ensures that the adsorption of an analyte at the surface of the nanowire leads to large changes in carrier mobility since the surface of the nanowire forms a large fraction of the bulk of the nanowire. Using this strategy, pH, protein, DNA and virus sensors have been fabricated with extremely high sensitivity e.g. electrical detection of 10fM concentration of DNA. For detection of biological moieties such as viruses, it is sometimes necessary to functionalize the nanowire surface using molecular receptors such as antibodies. For example, virus solutions with concentrations of 10^{-18} M bound to p-type Si nanowire devices (modified with the monoclonal antibody for influenza) and produced well-defined discrete detectable conductance changes.

5.3. *Photonics*

Nanowires fabricated with III–V and II–VI direct band gap semiconductors have been used as building blocks to produce multicolor, electrically driven nanophotonic systems [132–140]. Moreover due to their anisotropic geometry, as noted by Duan *et al.* [136], when single crystal nanowires are used with flat ends, the nanowire itself can behave as a Fabry-Perot optical cavity with modes $m\frac{\lambda}{2n_1} = L$, where m is an integer and L is the length of the nanowire. Since the light is constrained to within the nanowire, the nanowires were noted [136] to function as efficient lasing structures. These nanowire lasers were demonstrated using an n-type CdS nanowire laser cavity assembled onto p-Si electrodes (see Fig. 9). The structure produced an n-CdS nanowire/p-Si heterojunction similar to a p-n diode that was used for injection. Images of room temperature electroluminescence produced in forward bias from these hybrid nanowire structures exhibited strong emission with narrow lasing lines. In reverse bias, nanowire light emitting diodes can function as photodiodes which were reported [139] to offer polarization dependent ultrasensitive detection

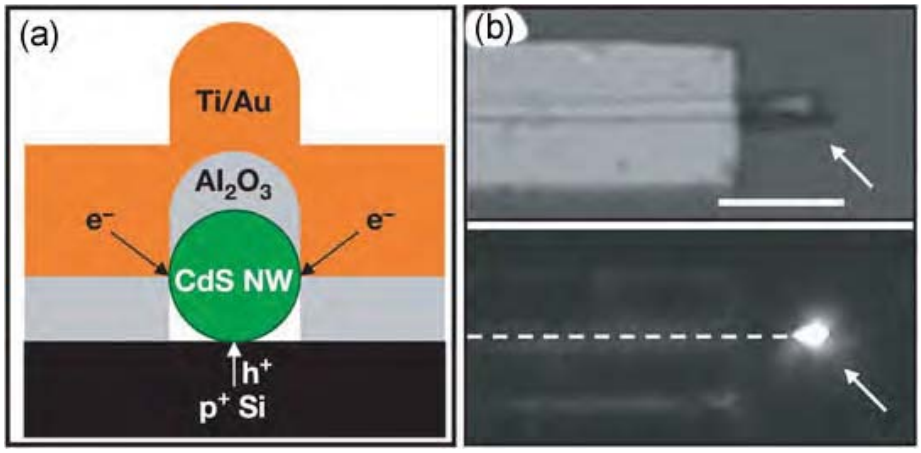

Figure 9. (a) Schematic showing the cross-section of a nanowire electrical injection laser. The devices were fabricated by assembling CdS nanowires on heavily doped p-Si on insulator substrates, followed by electron beam lithography and electron-beam evaporation of aluminium oxide, Ti and Au. One end of the nanowire was left uncovered for emission output from the device. (b) Top panel shows an optical image of a nanowire laser device. The arrow highlights the exposed CdS nanowire end. Scale bar is 5 μm. Bottom panel shows an electroluminescence image recorded from this device at room temperature with an injection current of about 80 mA. The arrow highlights emission from the CdS nanowire end. The dashed line highlights the nanowire position. Reprinted with permission from [136] by Nature Publishing Group.

limits of ∼100 photons with unprecedented spatial resolution of 250 nm × 250 nm. As compared to planar devices, a clear advantage of nanowire-based optical structures is the ability to combine ultrapure, single crystalline materials to achieve the required device function. By varying the chemical composition of different nanowires materials and junctions it is possible to create nanoscale light emitting sources and detectors emitting at different wavelengths.

5.4. *Solar Cells*

Dense arrays of oriented, crystalline dye sensitized zinc oxide nanowires have been used to fabricate solar cells (see Fig. 10) [141]. As opposed to thick films of zinc oxide or nanoparticle films, the advantage of using a nanowire film includes high internal surface area and direct electrical connections between nanowires for efficient and rapid carrier collection in the device. The full Sun efficiency of 1.5% was demonstrated. A switch from particles to wires also improved the charge transfer rates at the dye-semiconductor interfaces, due to a high number of single crystal planes, accounting for 95% of the surface area of the wires.

6. Defects and Errors

One of the big issues in self-assembly is that the structures that result have defects in them. At the present time, since the methodology of self-assembly is still in its infancy, quantitative studies on yield and reliability of structures have largely been

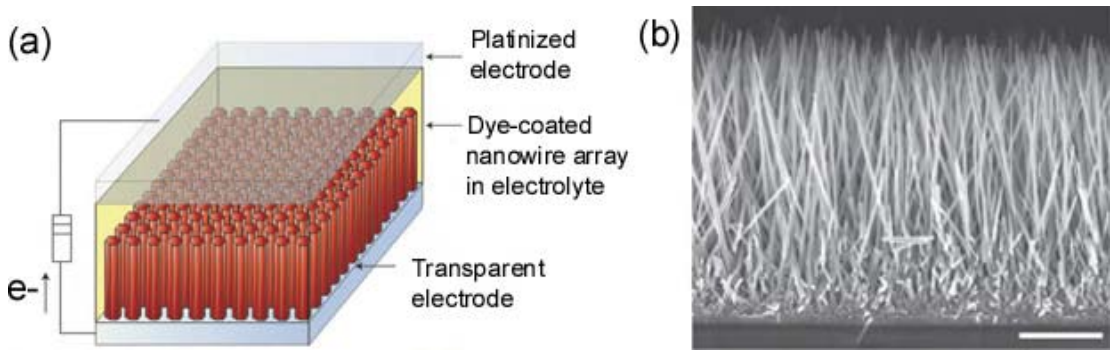

Figure 10. (a) Schematic of the nanowire dye-sensitized cell based on a ZnO nanowire array. Light is incident through the bottom electrode. (b) Typical SEM cross-section of a cleaved nanowire array on F:SnO_2 conductive glass (FTO). The nanowires are in direct contact with the substrate, with no intervening particle layer. Scale bar is 5 μm. Reprinted with permission from [141] by Nature Publishing Group.

ignored. As the methodology of fluidic assembly matures, it will be crucial that yields are quantified. Along with the identification of predominant defect modes, it is necessary to design assemblies that are inherently defect resistant. One strategy involves minimizing unfavorable interactions and maximizing favorable ones. In essence, it is necessary to design energy landscapes that are smooth, with a large funnel shaped global energy minimum, so that erroneous assemblies do not form as a result of the structure being trapped in a weak local minimum. An example of such a design was used in the demonstration of millimeter scale 3D networks by self-assembly [75]. In that case it was necessary to use patterns of solder dots on square faces of polyhedra to form electrical connections. Every pattern of solder dots results in a different energy landscape for the self-assembly. As an example, two patterns investigated are shown in Fig. 11 (a–b). The two patterns have four-fold rotational symmetry, but due to the enhanced local asymmetry of pattern *b*, a much smoother potential energy landscape results. When experiments were done with the pattern in Fig. 11(a), several erroneous attachments were observed including those in which only one dot on the mating faces was bonded. When patterns such as those in Fig. 11(b) were used, perfect assembly was obtained. A simulation of the energy landscape is shown in Fig. 11(c) [142]. There is a large global minimum and relatively weak local minima. It is believed that biological self-assembly such as protein folding, that occurs with incredible fidelity, is based on such funnel shaped potential energy landscapes.

It is possible to have structures function at the system level even in the presence of defects. For example, the fault tolerant system developed at Hewlett Packard [143] had 220,000 defects, demonstrating that it may be feasible to utilize and assemble chemical components with considerable defects, and still construct a functional computational network. Systems and architectures [143–146] that display this feature are called fault or defect tolerant. One of the easiest ways to incorporate defect tolerance into a system is to increase redundancy. This redundancy implies that

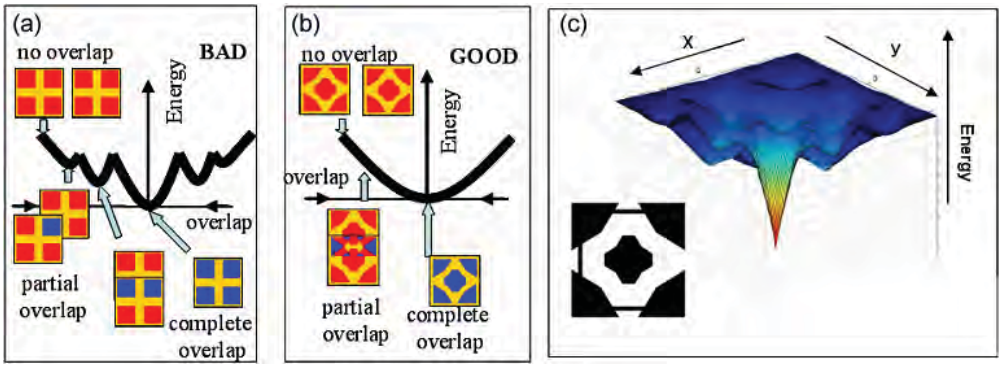

Figure 11. The design of energy landscapes for self-assembly that minimize errors. For binding between solder dots on square faces, a pattern of dots in (b) results in less errors than that shown in (a). This decrease in errors is due to the fact that the potential energy surface that results is smoother, with a larger global minimum and relatively weak local minima. (c) The actual surface energy plotted as a function of displacement in the plane of the pattern for assembly of two faces. Reprinted with permission from [142] by the Institute for Electrical and Electronics Engineers, Inc.. As can be seen, there exists a strong funnel shaped global minimum.

there exist multiple connections that serve the same function. Scale free network architectures are also inherently more robust and defect tolerant (see Fig. 12) [143].

Finally it is also possible to incorporate error correction schemes after integration using pick and place tools. However, it should be noted that this process will be serial and expensive.

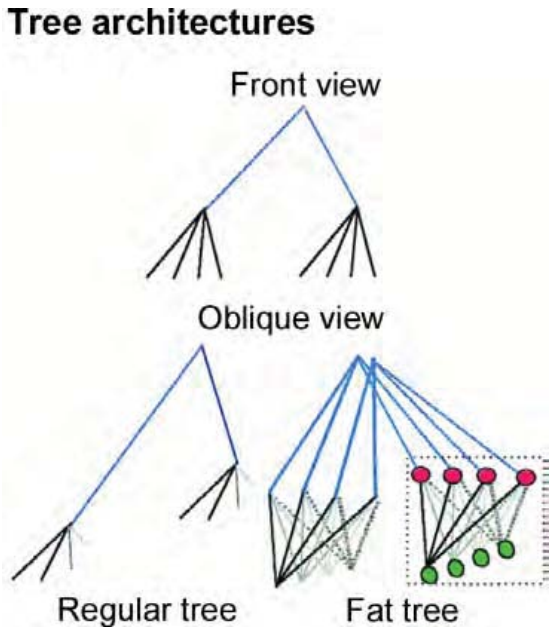

Figure 12. Schematic of a "fat tree" architecture. Reprinted with permission from [147] by The American Association for the Advancement of Science.

7. Conclusions and Perspective

In summary, nanowires are attractive building blocks for the fabrication of nanoscale electronics and devices. Various techniques are available for the facile fabrication of functional nanowire building blocks such as diodes and field effect transistors. Directed assembly and controlled growth are attractive bottom-up strategies to assemble the nanowires into functional devices. The critical challenges involve improving device to device variability, yields and defect tolerance. Moreover, studies need to be done to test reliability of these nanowire devices before they can be fully implemented. However, as an alternative to expensive top down methods for fabricating nanoscale devices, nanowire assembly and integration from bottom-up will continue to offer a promising alternative.

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References

1. J. Hu, T. W. Odom and C. M. Lieber, Chemistry and physics in one dimension: synthesis and properties of nanowires and nanotubes, *Acc. Chem. Res.*, **32**, 435–445 (1999).
2. Y. Wu, H. Yan, M. Huang, B. Messer, J. H. Song and P. Yang, Inorganic semiconductor nanowires: rational growth, assembly, and novel properties, *Chem. Eur. J.*, **8**, 1260–1268 (2002).
3. N. I. Kovtyukhova and T. E. Mallouk, Nanowires as building blocks for self-assembling logic and memory circuits, *Chem. Eur. J.*, **8**, 4354–4363 (2002).
4. P. Yang, Y. Wu and R. Fan, Inorganic semiconductor nanowires, *Int. J. Nanosci.*, **1**, 1–40 (2002).
5. Y. Xia, P. Yang, Y. Sun, Y. Wu, B. Mayers, B. Gates, Y. Yin, F. Kim and H. Yan, One-dimensional nanostructures: synthesis, characterization, and applications, *Adv. Mater.*, **5**, 353–389 (2003).
6. C. Lieber, Nanoscale science and technology: building a big future from small things, *MRS Bull.* **28**, 486–491 (2003).
7. M. Law, J. Goldberger and P. Yang, Semiconductor Nanowires and Nanotubes, *Annu. Rev. Mater. Res.*, **34**, 83–122 (2004).
8. Z. L. Wang, Zinc oxide nanostructures: growth, properties and applications, *J. Phys.: Condens. Matter,* **16**, R829–R858 (2004).
9. Y. Huang and C. M. Lieber, Integrated nanoscale electronics and optoelectronics: exploring nanoscale science and technology through semiconductor nanowires, *Pure Appl. Chem.*, **76**, 2051–2068 (2004).
10. C. J. Murphy, T. K. Sau, A. M. Gole, C. J. Orendorff, J. Gao, L. Gou, S. E. Hunyadi and T. Li, Anisotropic metal nanoparticles: synthesis, assembly and optical Applications, *J. Phys. Chem. B*, **109**, 13857–13870 (2005).

11. P. Yang, The chemistry and physics of semiconductor nanowires, *MRS Bull.*, **30**, 85–91 (2005)
12. J. Goldberger, R. Fan and P. Yang, Inorganic nanotubes: a novel platform for nanofluidics, *Acc. Chem. Res.*, **39**, 239–248 (2006).
13. S. J. Hurst, E. K. Payne, L. Qin and C. A. Mirkin, Multisegmented one-dimensional nanorods prepared by hard-template synthetic methods, *Angew. Chem. Int. Ed.*, **45**, 2672–2692 (2006).
14. S. Park, S.-W. Chung and C. A. Mirkin, Hybrid organic-inorganic, rod-shaped nanoresistors and diodes, *J. Am. Chem. Soc.*, **126**, 11772–11773 (2004).
15. Y. Wu and P. Yang, Direct observation of vapor-liquid-solid nanowire growth, *J. Am. Chem. Soc.*, **123**, 3165–3166 (2001).
16. E. A. Stach, P. J. Pauzauskie, T. Kuykendall, J. Goldberger, R. He and P. Yang, Watching GaN nanowires grow, *Nano Lett.*, **3**, 867–869 (2003).
17. S. Sharma, T. I. Kamins and R. S. Williams, Diameter control of Ti-catalyzed silicon nanowires, *J. Cryst. Growth*, **267**, 613–618 (2004).
18. P. X. Gao and Z. L. Wang, Substrate atomic-termination induced anisotropic growth of ZnO nanowires/nanorods by VLS process, *J. Phys. Chem. B*, **108**, 7534–7537 (2004).
19. S. Sharma, T. I. Kamins and R. S. Williams, Synthesis of thin silicon nanowires using gold-catalyzed chemical vapor deposition, *Appl. Phys. A*, **80**, 1225–1229 (2005).
20. J. H. He, C. S. Lao, L. J. Chen, D. Davidovic and Z. L. Wang, Large-scale Ni-doped ZnO nanowire arrays and electrical and optical properties, *J. Am. Chem. Soc.*, **127**, 16376–16377 (2005).
21. I. Lombardi, A. I. Hochbaum, P. Yang, C. Carraro and R. Maboudian, Synthesis of high density, size-controlled Si nanowire arrays via porous anodic alumina mask, *Chem. Mater.*, **18**, 988–991 (2006).
22. J. H. He, T. H. Wu, C. L. Hsin, K. M. Li, L. J. Chen, Y. L. Chueh, L. J. Chou and Z. L. Wang, Beaklike SnO_2 nanorods with strong photoluminescent and field-emission properties, *Small*, **2**, 116–120 (2006).
23. L. J. Lauhon, M. S. Gudiksen, D. Wang and C. M. Lieber, Epitaxial core–shell and core–multishell nanowire heterostructures, *Nature*, **420**, 57–61 (2002).
24. T. Hanrath and B. Korgel, Supercritical fluid-liquid-solid (SFLS) synthesis of Si and Ge nanowires seeded by colloidal metal nanocrystals, *Adv. Mater.*, **15**, 437–440 (2005).
25. H.-Y. Tuan, D. C. Lee, T. Hanrath and B. A. Korgel, Germanium nanowire synthesis: an example of solid-phase seeded growth with nickel nanocrystals, *Chem. Mater.*, **17**, 5705–5711 (2005).
26. H.-Y. Tuan, D. C. Lee, T. Hanrath and B. A. Korgel, Catalytic solid-phase seeding of silicon nanowires by nickel nanocrystals in organic solvents, *Nano Lett.*, **5**, 681–684 (2005).
27. T. J. Trentler, K. M. Hickman, S. C. Goel, A. M. Viano, P. C. Gibbons and W. E. Buhro, Solution-liquid-solid growth of crystalline III-V semiconductors: an analogy to vapor-liquid-solid growth, *Science*, **270**, 1791–1794 (1995).
28. H. Yu, J. Li, R. A. Loomis, P. C. Gibbons, L.-W. Wang and W. E. Buhro, Cadmium selenide quantum wires and the transition from 3D to 2D confinement, *J. Am. Chem. Soc.*, **125**, 16168–16169 (2003).
29. N. R. Jana, L. Gearheart and C. J. Murphy, Wet chemical synthesis of silver nanorods and nanowires of controllable aspect ratio, *Chem. Commun.*, 617–618 (2001).

30. J. Gao, C. M. Bender and C. J. Murphy, Dependence of the gold nanorod aspect ratio on the nature of the directing surfactant in aqueous solution, *Langmuir*, **19**, 9065–9070 (2003).
31. Y. Sun, B. Mayers, T. Herricks and Y. Xia, Polyol synthesis of uniform silver nanowires: a plausible growth mechanism and the supporting evidence, *Nano Lett.*, **3**, 955–960 (2003).
32. C. Qian, F. Kim, L. Ma, F. Tsui, P. Yang and J. Liu, Solution-phase synthesis of single-crystalline iron phosphide nanorods/nanowires, *J. Am. Chem. Soc.*, **126**, 1195–1198 (2004).
33. T. K. Sau and C. J. Murphy, Seeded high yield synthesis of short Au nanorods in aqueous solution, *Langmuir*, **20**, 6414–6420 (2004).
34. L. Gou and C. J. Murphy, Fine-tuning the shape of gold nanorods, *Chem. Mater.*, **17**, 3669–3673 (2005).
35. C. R. Martin, Membrane-based synthesis of nanomaterials, *Chem. Mater.*, **8**, 1739–1746 (1996).
36. V. M. Cepak and C. R. Martin, Preparation of polymeric micro- and nanostructures using a template-based deposition method, *Chem. Mater.*, **11**, 1363–1367 (1999).
37. S. Demoustier-Champagne and P.-Y. Stavaux, Effect of electrolyte concentration and nature on the morphology and the electrical properties of electropolymerized polypyrrole nanotubules, *Chem. Mater.*, **11**, 829–834 (1999).
38. M. Steinhart, J. H. Wendorff, A. Greiner, R. B. Wehrspohn, K. Nielsch, J. Schilling, J. Choi and U. Gosele, Polymer Nanotubes by Wetting of Ordered Porous Templates, *Science*, **296**, 1997 (2002).
39. Y. Long, Z. Chen, N. Wang, Y. Ma, Z. Zhang, L. Zhang and M. Wan, Electrical conductivity of a single conducting polyaniline nanotube, *Appl. Phys. Lett.*, **83**, 1863–1865 (2003).
40. M. Chen, P. C. Searson and C. L. Chien, Micromagnetic behavior of electrodeposited Ni/Cu multilayer nanowires, *J. Appl. Phys.,* **93**, 8253–8255 (2003).
41. C. Ji and P. C. Searson, Synthesis and characterization of nanoporous gold nanowires, *J. Phys. Chem. B*, **107**, 4494–4499 (2003).
42. P. W. Gibson, H. L. Schreuder-Gibson and D. Rivin, Electrospun fiber mats: transport properties, *AIChE J.*, **45**, 190–195 (1999).
43. I. D. Norris, M. M. Shaker, F. K. Ko and A. G. MacDiarmid, Electrostatic fabrication of ultrafine conducting fibers: polyaniline polyethylene oxide blends, *Synth. Met.*, **114**, 109–114 (2000).
44. J. Kameoka and H. G. Craighead, Fabrication of oriented polymeric nanofibers on planar surfaces by electrospinning, *Appl. Phys. Lett.*, **83**, 371–373 (2003).
45. D. Li, Y. Wang and Y. Xia, Electrospinning nanofibers as uniaxially aligned arrays and layer-by-layer stacked films, *Adv. Mater.*, **16**, 361–366 (2004).
46. X. Lu, Y. Zhao, C. Wang and Y. Wei, Fabrication of CdS nanorods in PVP fiber matrices by electrospinning, *Macromol. Rapid Commun.*, **26**, 1325–1329 (2005).
47. X. Lu, D. Zhang, Q. Zhao, C. Wang, W. Zhang and Y. Wei, Large-scale synthesis of necklace-like single-crystalline PbTiO3 nanowires, *Macromol. Rapid Commun.*, **27**, 76–80 (2006).
48. K. H. Hong and T. J. Kang, Polyaniline–Nylon 6 composite nanowires prepared by emulsion polymerization and electrospinning process, *J. Appl. Polym. Sci.*, **99**, 1266–1286 (2006).
49. Y.-T. Jia, H.-Y. Kim, J. Gong and D.-R. Lee, Electrospun nanofibers of block copolymer of trimethylene carbonate and ε-caprolactone, *J. Appl. Polym. Sci.*, **99**, 1462–1470 (2006).

50. A. M. Morales and C. M. Lieber, A laser ablation method for the synthesis of crystalline semiconductor nanowires, *Science*, **279**, 208–211 (1998).
51. A. Kotlyar, N. Borovok, T. Molotsky, H. Cohen, E. Shapir and D. Porath, Long, monomolecular Gyanine-based nanowires, *Adv. Mater.*, **17**, 1901–1905 (2005).
52. S. Hou, J. Wang and C. R. Martin, Template-synthesized DNA nanotubes, *J. Am. Chem. Soc.*, **127**, 8586–8587 (2005).
53. Q. Gu, C. Cheng, R. Gonela, S. Suryanarayanan, S. Anabathula, K. Dai1 and D. T. Haynie, DNA nanowire fabrication, *Nanotechnology*, **17**, R14-R25 (2006).
54. K. T. Nam, D.-W. Kim, P. J. Yoo, C.-Y. Chiang, N. Meethong, P. T. Hammond, Y.-M. Chiang and A. M. Belcher, Virus-enabled synthesis and assembly of nanowires for lithium ion battery electrodes, *Science*, **312**, 885–888 (2006).
55. S. Hsieh, S. Meltzer, C. R. C. Wang, A. A. G. Requicha, M. E. Thompson and B. E. Koel, Imaging and manipulation of gold nanorods with an atomic force microscope, *J. Phys. Chem. B*, **106**, 231–234 (2002).
56. Y. Chen, D. A. A. Ohlberg, G. Medeiros-Ribeiro, Y. A. Chang and R. S. Williams, Self-assembled growth of epitaxial erbium disilicide nanowires on silicon (001), *Appl. Phys. Lett.*, **76**, 4004–4006 (2000).
57. Y. Chen, D. A. A. Ohlberg and R. S. Williams, Nanowires of four epitaxial hexagonal silicides grown on Si(001), *J. Appl. Phys.*, **91**, 3213–3219 (2002).
58. R. Ragana, Y. Chena, D. A. A. Ohlberga, G. Medeiros-Ribeirob and R. S. Williams, Ordered arrays of rare-earth silicide nanowires on Si(001), *J. Cryst. Growth*, **251**, 657–661 (2003).
59. P. Nguyen, H. T. Ng, J. Kong, A. M. Cassell, R. Quinn, J. Li, J. Han, M. McNeil and M. Meyyappan, Epitaxial directional growth of indium-doped tin oxide nanowire arrays, *Nano Lett.*, **3**, 925–928 (2003).
60. D. F. Moore, Y. Ding and Z. L. Wang, Crystal orientation-ordered ZnS nanowire bundles, *J. Am. Chem. Soc.*, **126**, 14372–14373 (2004).
61. T. L. Karmins, X. Li and R. S. Williams, Growth and structure of chemically vapor deposited Ge nanowires on Si substrates, *Nano Lett.*, **4**, 503–506 (2004).
62. M. S. Islam, S. Sharma, T. I. Kamins and R. S. Williams, Ultrahigh-density silicon nanobridges formed between two vertical silicon surfaces, *Nanotechnology*, **15**, 15–18 (2004).
63. T. Kuykendall, P. J. Pauzauskie1, Y. Zhang, J. Goldberger1, D. Sirbuly, J. Denlinger and P. Yang, Crystallographic alignment of high-density gallium nitride nanowire arrays, *Nature*, **3**, 524–528 (2004).
64. R. He, D. Gao, R. Fan, A. I. Hochbaum, C. Carraro, R. Maboudian and P. Yang, Si nanowire bridges in microtrenches: integration of growth into device fabrication, *Adv. Mater.*, **17**, 2098–2102 (2005).
65. X. Wang, J. Song, P. Li, J. H. Ryou, R. D. Dupuis, C. J. Summers and Z. L. Wang, Growth of uniformly aligned ZnO nanowire heterojunction arrays on GaN, AlN, and Al0.5Ga0.5N substrates, *J. Am. Chem. Soc.*, **127**, 7920–7923 (2005).
66. S. Sharma, T. I. Kamins, M. S. Islam, R. S. Williams and A. F. Marshall, Structural characteristics and connection mechanism of gold-catalyzed bridging silicon nanowires, *J. Cryst. Growth*, **280**, 562–568 (2005).
67. X. Wen, S. Wang, Y. Ding, Z. L. Wang and S. Yang, Controlled growth of large-area, uniform, vertically aligned arrays of r-Fe_2O_3 nanobelts and nanowires, *J. Phys. Chem. B*, **109**, 215–220 (2005).
68. J. Song, X. Wang, E. Riedo and Z. L.Wang, Systematic study on experimental conditions for large-scale growth of aligned ZnO nanwires on nitrides, *J. Phys. Chem. B*, **109**, 9869–9872 (2005).

69. A. I. Hochbaum, R. Fan, R. He and P. Yang, Controlled growth of Si nanowire arrays for device integration, *Nano Lett.*, **5**, 457–460 (2005).
70. L. E. Greene, M. Law, D. H. Tan, M. Montano, J. Goldberger, G. Somorjai and P. Yang, General route to vertical ZnO nanowire arrays using textured ZnO seeds, *Nano Lett.*, **5**, 1231–1236 (2005).
71. D. Gao, R. He, C. Carraro, R. T. Howe, P. Yang and R. Maboudian, Selective growth of Si nanowire arrays via galvanic displacement processes in water-in-oil microemulsions, *J. Am. Chem. Soc.*, **127**, 4574–4575 (2006).
72. J. H. He, J. H. Hsu, C. H. Wang, H. N. Lin, L. J. Chen and Z. L. Wang, Pattern and feature designed growth of ZnO nanowire arrays for vertical devices, *J. Phys. Chem. B*, **110**, 50–53 (2006).
73. G. M. Whitesides and M. Boncheva, Beyond molecules: self-assembly of mesoscopic and macroscopic components, *Proc. Nat. Acad. Sci. USA*, **99**, 4769–4774 (2002).
74. S. R. J. Oliver, N. Bowden and G. M. Whitesides, Self-assembly of hexagonal rod arrays based on capillary forces, *J. Colloid Interface Sci.*, **224**, 425–428 (2000).
75. D. H. Gracias, J. Tien, T. L. Breen, C. Hsu and G. M. Whitesides, Forming electrical networks in three dimensions by self-assembly, *Science*, **289**, 1170–1172 (2000).
76. H. O. Jacobs, A. R. Tao, A. Schwartz, D. H. Gracias and G. M. Whitesides, Fabrication of a cylindrical display by patterned assembly, *Science*, **296**, 323–325 (2002).
77. S. Park, J.-H. Lim, S.-W. Chung and C. A. Mirkin, Self-assembly of mesoscopic metal-polymer amphiphiles, *Science* **303**, 348–351 (2004).
78. J. K. N. Mbindyo, B. D. Reiss, B. R. Martin, C. D. Keating, M. J. Natan and T. E. Mallouk, DNA-directed assembly of gold nanowires on complimentary surfaces, *Adv. Mater.*, **13**, 249–254 (2001).
79. K. K. Caswell, J. N. Wilson, U. H. F. Bunz and C. J. Murphy, Preferential end-to-end assembly of gold nanorods by biotin-streptavidin connectors, *J. Am. Chem. Soc.*, **125**, 13914–13915 (2003).
80. Z. Deng and C. Mao, DNA-templated fabrication of 1D parallel and 2D crossed metallic nanowire arrays, *Nano Lett.*, **3**, 1545–1548 (2003).
81. A. K. Salem, J. Chao, K. W. Leong and P. C. Searson, Receptor-mediated self-assembly of multi-component magnetic nanowires, *Adv. Mater.*, **16**, 268–271 (2004).
82. A. K. Salem, M. Chen, J. Hayden, K. W. Leong and P. C. Searson, Directed assembly of multisegment Au/Pt/Au nanowires, *Nano Lett.*, **4**, 1163–1165 (2004).
83. A. Gole and C. J. Murphy, Biotin-streptavidin-induced aggregation of gold nanorods: tuning rod-rod orientation, *Langmuir*, **21**, 10756–10762 (2005).
84. Q. Zhang, S. Gupta, T. Emrick and T. P. Russell, Surface-functionalized CdSe nanorods for assembly in diblock copolymer templates, *J. Am. Chem. Soc.*, **128**, 3898–3899 (2006).
85. M. Chen, L. Guo, R. Ravi and P. C. Searson, Kinetics of receptor directed assembly of multisegment nanowires, *J. Phys. Chem. B*, **110**, 211–217 (2006).
86. A. A. Wang, J. Lee, G. Jenikova, A. Mulchandani, N. V. Myung and W. Chen, Controlled assembly of multi-segment nanowires by histidine-tagged peptides, *Nanotechnology*, **17**, 3375–3379 (2006).
87. A. Pohl, *Dielectrophoresis: The Behavior of Neutral Matter in Nonuniform Electric Fields,* Cambridge University Press, Cambridge, New York, 1978.
88. P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo and T. E. Mallouk, Electric-field assisted assembly and alignment of metallic nanowires, *Appl. Phys. Lett.*, **77**, 1399–1301 (2000).

89. A. Theron, E. Zussman1 and A. L. Yarin, Electrostatic field-assisted alignment of electrospun nanofibres, *Nanotechnology*, **12**, 384–390 (2001).
90. X. Duan, Y. Huang, Y. Cui, J. Wang and C. M. Lieber, Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices, *Nature*, **409**, 66–69 (2001).
91. D. L. Fan, F. Q. Zhu, R. C. Cammarata and C. L. Chien, Manipulation of nanowires in suspension by ac electric fields, *Appl. Phys. Lett.*, **85**, 4175–4178 (2004).
92. C. Cheng, R. K. Gonela, Q. Gu and D. T. Haynie, Self-assembly of metallic nanowires from aqueous solution, *Nano Lett.*, **5**, 175–178 (2005).
93. O. Englander, D. Christensen, J. Kim, L. Lin and S. J. S. Morris, Electric-field assisted growth and self-assembly of intrinsic silicon nanowires, *Nano Lett.*, **5**, 705–708 (2005).
94. J. J. Boote and S. D. Evans, Dielectrophoretic manipulation and electrical characterization of gold nanowires, *Nanotechnology*, **16**, 1500–1505 (2005).
95. S. J. Papadakis, Z. Gu and D. H. Gracias, Dielectrophoretic assembly of reversible and irreversible metal nanowire networks and vertically aligned arrays, *Appl. Phys. Lett.*, **8**, 233116 (2006).
96. Y. Liu, J.-H. Chung, W. K. Liu and R. S. Ruoff, Dielectrophoretic assembly of nanowires, *J. Phys. Chem. B*, **110**, 14098–14106 (2006).
97. C. S. Lao, J. Liu, P. X. Gao, L. Zhang, D. Davidovic, R. Tummala and Z. L. Wang, ZnO nanobelt/nanowire Schottky diodes formed by dielectrophoresis alignment across Au electrodes, *Nano Lett.*, **6**, 263–266 (2006).
98. K. M. Ryan, A. Mastroianni, K. A. Stancil, H. Liu and A. P. Alivisatos, Electric-field-assisted assembly of perpendicularly oriented nanorod superlattices, *Nano Lett.*, **6**, 1479–1482 (2006).
99. M. Tanase, L. A. Bauer, A. Hultgren, D. M. Silevitch, L. Sun, D. H. Reich, P. C. Searson and G. J. Meyer, Magnetic alignment of fluorescent nanowires, *Nano Lett.,* **1**, 155–158 (2001).
100. M. Tanase, D. M. Silvitch, A. Hultgren, L. A. Bauer, P. C. Searson, G. J. Meyer and D. H. Reich, Magnetic trapping and self-assembly of multicomponent nanowires, *J. App. Phys.*, **91**, 8549–8552 (2002).
101. C. L. Chien, L. Sun, M. Tanase, L. A. Bauer, A. Hulgren, D. M. Silevitch, G. J. Meyer, P. C. Searson and D. H. Reich, Electrodeposited magnetic nanowires: arrays, field-induced assembly and surface functionalization, *J. Magn. Magn. Mater.,***249**, 146-155 (2002).
102. J. C. Love, A. R. Urbach, M. G. Prentiss and G. M. Whitesides, Three-dimensional self-assembly of metallic rods with submicron diameters using magnetic interactions, *J. Am. Chem. Soc.*, **125**, 12696–12697 (2003).
103. C. M. Hangarter and N. V. Myung, Magentic alignment of nanowires, *Chem. Mater.*, **17**, 1320–1324 (2005).
104. E. Choi, Z. Gu, D. Gracias and A. G. Andreou, Chip-scale magnetic sensing and control of nanoparticles and nanorods, *2006 IEEE International Symposium on Circuits and Systems (ISCAS 2006)*, 1319–1322 (2006).
105. H. Ye, Z. Gu, T. Yu and D. H. Gracias, Integrating nanowires with substrates using directed assembly and nanoscale soldering, *IEEE Trans. Nanotechnol.*, **5**, 62–66 (2006).
106. B. Yoo, Y. Rheem, W. P. Beyermann and N. V. Myung, Magnetically assembled 30 nm diameter nickel nanowire with ferromagnetic electrodes, *Nanotechnology*, **17**, 2512–2517 (2006).

107. R. Agarwal, K. Ladavac, Y. Roichman, G. Yu, C. M. Lieber and D. G. Grier, Manipulation and assembly of Nanowires with holographic optical traps, *Opt. Exp.*, **13**, 8906–8912 (2005).
108. P. J. Pauzauskie1, A. Radenovic, E. Trepagnier, H. Shroff, P. Yang and J. Liphardt, Optical trapping and integration of semiconductor nanowire assemblies in water, *Nature*, **5**, 97–101 (2006).
109. F. Kim, S. Kwan, J. Akana and P.Yang, Langmuir-Blodgett nanorod assembly, *J. Am. Chem. Soc.*, **123**, 4360-4361 (2001).
110. P. Yang and F. Kim, Langmuir-Blodgett assembly of one-dimensional nanostructures, *ChemPhysChem*, **3**, 503–506 (2002).
111. A. Tao, F. Kim, C. Hess, J. Goldberger, R. He, Y. Sun, Y. Xia and P. Yang, Langmuir-Blodgett silver nanowire monolayers for molecular sensing using surface-enhanced raman spectroscopy, *Nano Lett.*, **3**, 1229–1233 (2003).
112. D. Whang, S. Jin, Y. Wu and C. M. Lieber, Large-scale hierarchical organization of nanowire arrays for integrated nanosystems, *Nano Lett.*, **3**, 1255–1259 (2003).
113. P. Yang, Nanotechnology: wires on water, *Nature*, **425**, 243–244 (2003).
114. S. Acharya, A. B. Panda, N. Belman, S. Efrima and Y. Golan, A semiconductor-nanowire assembly of ultrahigh junction density by the Langmuir–Blodgett technique, *Adv. Mater.*, **18**, 210–213 (2006).
115. Z. Gu, Y. Chen and D. H. Gracias, Surface tension driven self-assembly of bundles and networks of 200 nm diameter rods using a polymerizable adhesive, *Langmuir*, **20**, 11308–11311 (2004).
116. Z. Gu, H. Ye and D. H. Gracias, The bonding of nanowire assemblies using adhesive and solder, *JOM*, 60–64 (2005).
117. S. Jin, D. Whang, M. C. McAlpine, R. S. Friedman, Y. Wu and C. M. Lieber, Scalable interconnection and integration of nanowire devices without registration, *Nano Lett.*, **4**, 915–919 (2004).
118. Z. Gu, H. Ye, D. Smirnova, D. Small and D. H. Gracias, Reflow and electrical characteristics of nanoscale solder, *Small*, **2**, 225–229 (2006).
119. N. I. Kovtyukhova, B. K. Kelley and T. E. Mallouk, Coaxially gated in-wire thin-film transistors made by template assembly, *J. Am. Chem. Soc.*, **126**, 12738–12739 (2004).
120. Y. Cui, Z. Zhong, D. Wang, W. U. Wang and C. M. Lieber, High performance silicon nanowire field effect transistors, *Nano Lett.*, **3**, 149–152 (2003).
121. P. Nguyen, H. T. Ng, T. Yamada, M. K. Smith, J. Li, J. Han and M. Meyyappan, Direct integration of metal oxide nanowire in vertical field-effect transistor, *Nano Lett.*, **4**, 651–657 (2004).
122. N. I. Kovtyukhova and T. E. Mallouk, Nanowire p-n heterojunction diodes made by templated assembly of multilayer carbon-nanotube/polymer/semiconductior-particle shells around metal nanowires, *Adv. Mater.*, **17**, 187–192 (2005).
123. J. Goldberger, D. J. Sirbuly, M. Law and P. Yang, ZnO nanowire transistors, *J. Phys. Chem. B*, **109**, 9–14 (2005).
124. J. Goldberger, A. I. Hochbaum, R. Fan and P. Yang, Silicon vertically integrated nanowire field effect transistors, *Nano Lett.*, **6**, 973–977 (2006).
125. Z. Li, B. Rajendran, T. I. Kamins, X. Li, Y. Chen and R. S. Williams, Silicon nanowires for sequence-specific DNA sensing: device fabrication and simulation, *Appl. Phys. A*, **80**, 1257–1263 (2005).
126. D. J. Sirbuly, M. Law, P. Pauzauskie, H. Yan, A. V. Maslov, K. Knutsen, C.-Z. Ning, R. J. Saykally and P. Yang, Optical routing and sensing with nanowire assemblies, *Proc. Nat. Acad. Sci. USA*, **102**, 7800–7805 (2005).

127. A. K. Wanekaya, W. Chen, N. V. Myung and A. Mulchandani, Nanowire-based electrochemical biosensors, *Electroanalysis*, **18**, 533–550 (2006).
128. F. Patolsky and C. M. Lieber, Nanowire sensors, *Mater. Today*, 20–28 (2005).
129. G. Zheng, F. Patolsky, Y. Cui, W. U. Wang and C. M. Lieber, Multiplexed electrical detection of cancer markers with nanowire sensor arrays, *Nat. Biotech.*, **23**, 1294–1301 (2005).
130. F. Patolsky, G. Zheng and C. M. Lieber, Nanowire-based biosensors, *Anal. Chem.*, **78**, 4260–4269 (2006).
131. F. Patolsky, G. Zheng and C. M. Lieber, Nanowire sensors for medicine and the life sciences, *Nanomedicine*, **1**, 51–65 (2006).
132. J. C. Johnson, H. Yan, R. D. Schaller, L. H. Haber, R. J. Saykally and P. Yang, Single nanowire lasers, *J. Phys. Chem. B*, **105**, 11387–11390 (2001).
133. M. H. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo and P. Yang, Room-temperature ultraviolet nanowire nanolasers, *Science*, **292**, 1897–1899 (2001).
134. H. Kind, H. Yan, B. Messer, M. Law and P. Yang, Nanowire ultraviolet photodetectors and optical switches, *Adv. Mater.* **14**, 158–160 (2002).
135. J. C. Johnson, H.-J. Choi, K. P. Knutsen, R. D. Schaller, P. Yang and R. J. Saykally, Single gallium nitride nanowire lasers, *Nature Mater.*, **1,** 106–110 (2002).
136. X. Duan, Y. Huang, R. Agarwal and C. M. Lieber, Single-nanowire electrically driven lasers, *Nature*, **421**, 241–246 (2003).
137. Y. Huang, X. Duan and C. M. Lieber, Nanowires for integrated multicolor nanophotonics, *Small*, **1**, 142–147 (2005).
138. D. J. Sirbuly, M. Law, H. Yan and P. Yang, Semiconductor nanowires for subwavelength photonics integration, *J. Phys. Chem. B*, **109**, 15190-15213 (2005).
139. O. Hayden, R. Agarwal and C. M. Lieber, Nanoscale avalanche photodiodes for highly sensitive and spatially resolved photon detection, *Nature*, **5**, 352–356 (2006).
140. P. J. Pauzauskie, D. J. Sirbuly and P. Yang, Semiconductor nanowire ring resonator laser, *Phys. Rev. Lett.*, **96**, 143903 (2006).
141. M. Law, L. E. Greene, J. C. Johnson, R. Saykally and P. Yang, Nanowire dye-sensitized solar cells, *Nature Mater.*, **4**, 455–459 (2005).
142. K. F. Bohringer, U. Srinivasan and R. T. Howe, Modeling of capillary forces and binding sites for fluidic self-assembly, *The 14th IEEE Int. Conf. MEMS*, 369–374 (2001).
143. J. R. Heath, P. J. Kuekes, G. S. Snider and R. S. Williams, A defect-tolerant computer architecture: opportunities for nanotechnology, *Science* **1998,** *280,* 1716–1721.
144. P. J. Kuekes, W. Robinett, G. Seroussi and R. S. Williams, Defect-tolerant demultiplexers for nano-electronics constructed from error-correcting codes, *Appl. Phys. A*, **80**, 1161–1164 (2005).
145. P. J. Kuekes, W. Robinett, G. Seroussi and R. S. Williams, Defect-tolerant interconnect to nanoelectronic circuits: internally redundant demultiplexers based on error-correcting codes, *Nanotechnology*, **16**, 869–882 (2005).
146. G. Snider, P. Kuekes, T. Hogg and R. S. Williams, Nanoelectronic architectures, *Appl. Phys. A*, **80**, 1183–1195 (2005).
147. R. Albert, H. Jeong and A.-L. Barabasi, Error and attack tolerance of complex networks, *Nature*, **406**, 378–382 (2000).